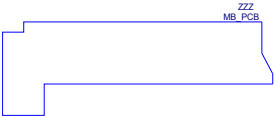


MODEL NAME : LA-C791P
PCB NO : DAA000AS000
BOM P/N :



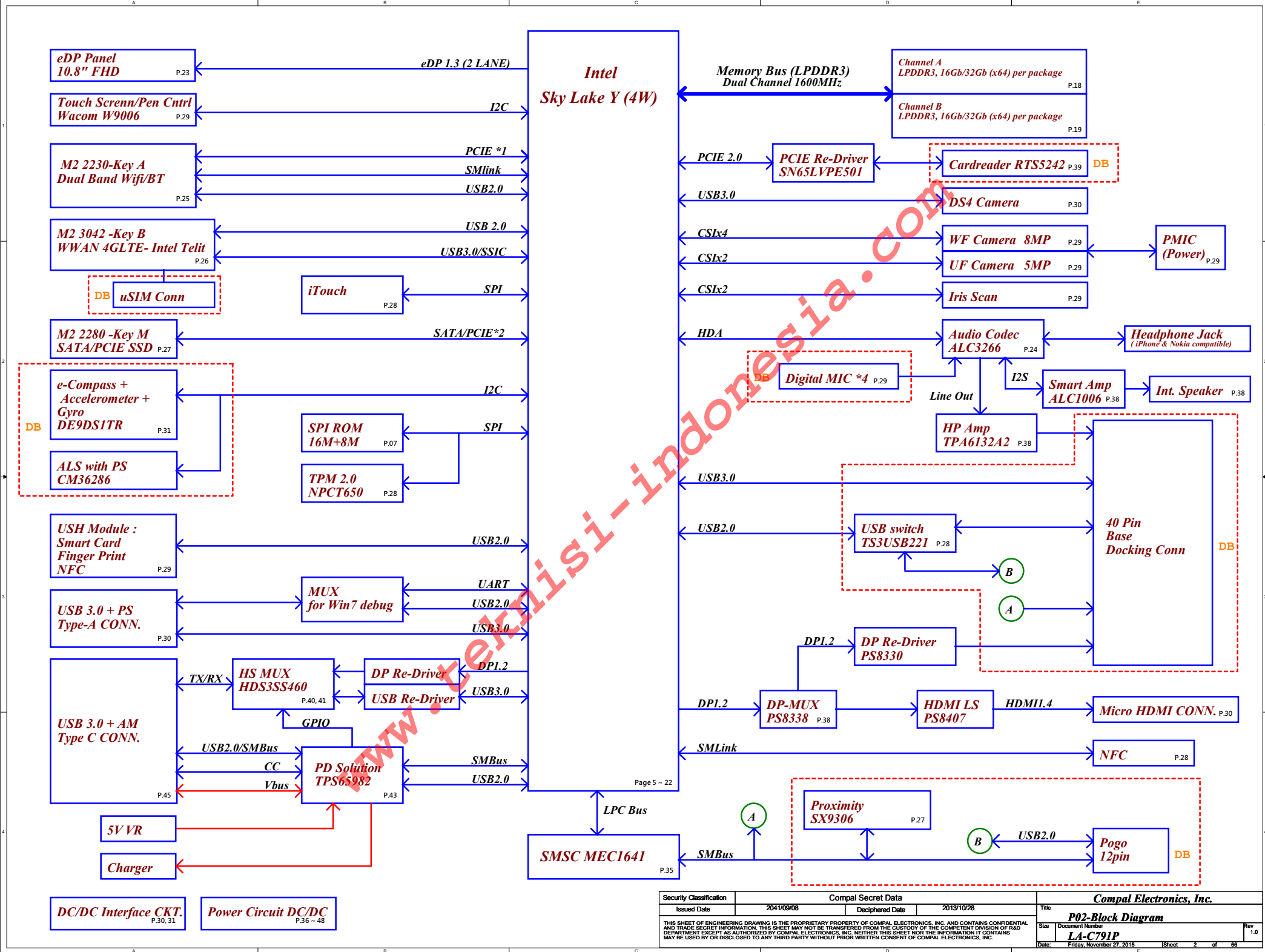
Dell/Compal Confidential

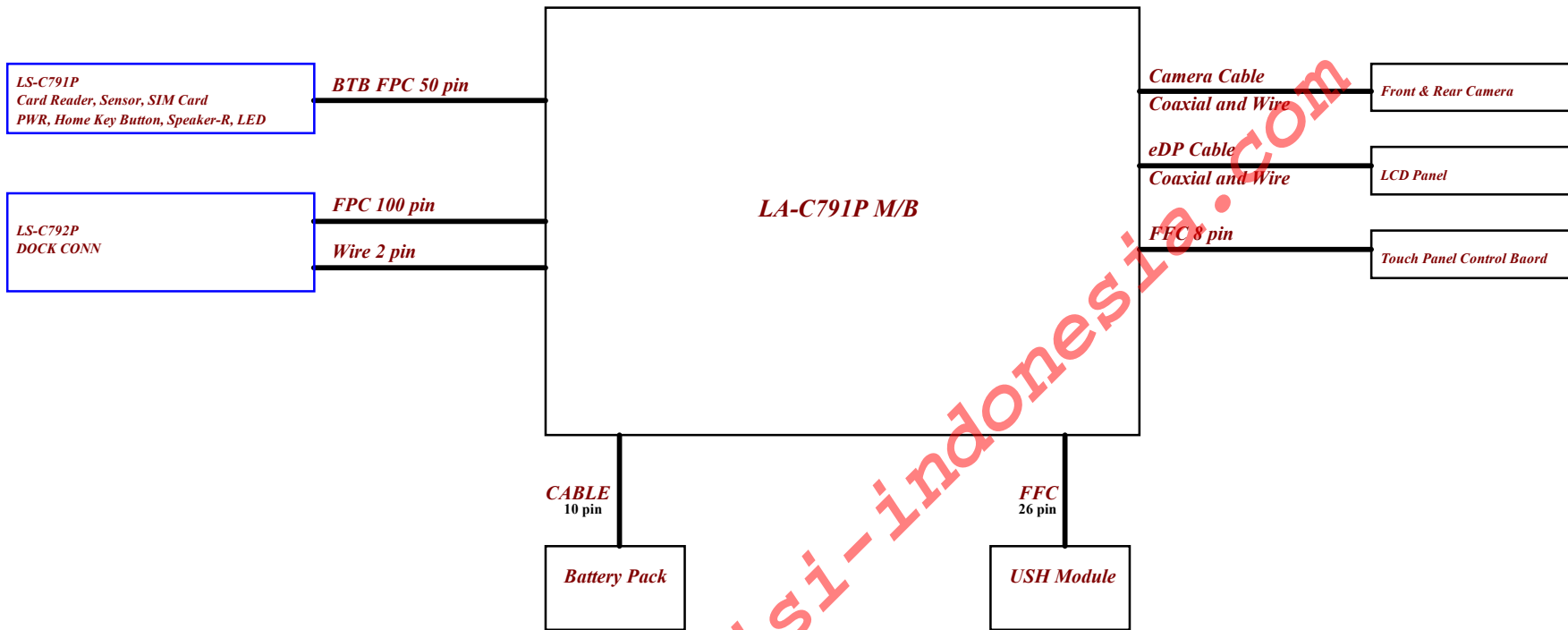
Schematic Document

Jayton 2 (Skylake Y)

2015-11-09
Rev: 1.0

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		P01-Cover Page				
		Size	Document Number			Rev
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				LA-C791P	1.0
		Date:		Friday, November 27, 2015	Sheet 3 of 65

Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	REV	
0	240K +/- 5%	4700p		
1	130K +/- 5%	4700p		
2	62K +/- 5%	4700p		
3	33K +/- 5%	4700p		
4	8.2K +/- 5%	4700p		
5	4.3K +/- 5%	4700p		
6	2K +/- 5%	4700p		
7	NC			

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	1.0
6	
7	

SMBUS Control Table

	SOURCE	Base	BATT	Charger	XDP	NFC	USH	PD Controller	Trinity Dock	P-Sensor
PCH_SMLCLK PCH_SMLDATA	PCH					V				
PCH_SMLCLK PCH_SMLDATA	PCH									
SMBCLK SMBDATA	PCH				V					
EC_SMB00_CLK EC_SMB00_DAT	MEC1641									
EC_SMB01_CLK EC_SMB01_DAT	MEC1641						V			V
EC_SMB03_CLK EC_SMB03_DAT	MEC1641		V							
EC_SMB04_CLK EC_SMB04_DAT	MEC1641			V						
EC_SMB05_CLK EC_SMB05_DAT	MEC1641	V								
EC_SMB07_CLK EC_SMB07_DAT	MEC1641							V	V	

Link

Flexible I/O	Interface	DESTINATION
1	USB 3.0 #1	USB Type-C
2	USB 3.0 #2/SSIC	NGFF (WWAN)
3	USB 3.0 #3	BASE
4	USB 3.0 #4	DS4 CAM
5	USB 3.0 #5	USB Type-A
6		
7		
8		
9		
10		
11	PCI-E #7/SATA #0	NGFF (SSD)
12	PCI-E #8	NGFF (SSD)
13	PCI-E #9	NGFF (WLAN)
14	PCI-E #10	Card Reader

USB 2.0 PORT#	DESTINATION
1	USB Type-C
2	BT
3	WWAN
5	BASE
7	USH
9	USB Type-A

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE1	
	CLKOUT_PCIE2	Card Reader
	CLKOUT_PCIE3	NGFF (SSD)
	CLKOUT_PCIE4	NGFF (WLAN)
	FLEX CLOCKS	DESTINATION
	CLKOUT_LPC_0	EC LPC
DDI	CLKOUT_LPC_1	Debug

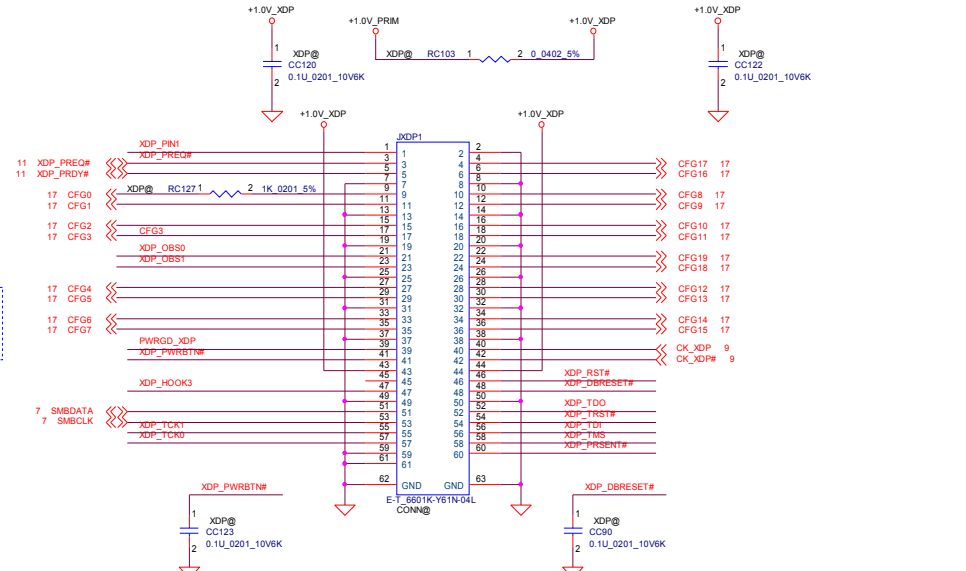
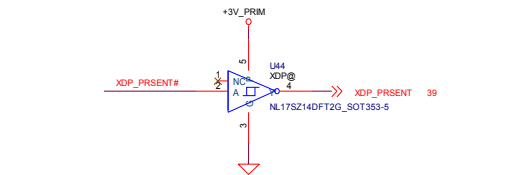
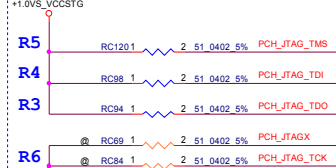
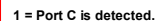
DDI	DDI PORT#	DESTINATION
	B	USB Type-C
	C	DP MUX

Symbol Note :

@ : means de-pop

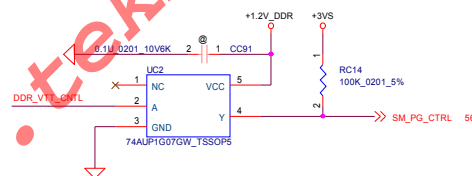
↓ : means Digital Ground

⏏ : means Analog Ground

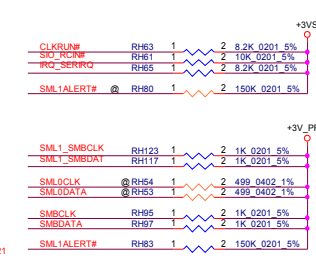


Security Classification	Compal Secret Data		Compal Electronics, Inc. P05-SKL Y(1/13) DDLMSIC.XDP	
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Un-nterleaved Memory



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Functional Strap Definitions

SMBALERT# / GPP_C2 (Internal Pull Down) :

TLS Confi-dentiality

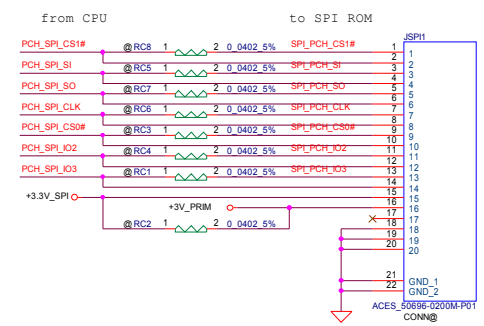
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).

1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

SML0ALERT# / GPP_C5 (Internal Pull Down) :

0 = LPC is selected for EC.

1 = eSPI is selected for EC.



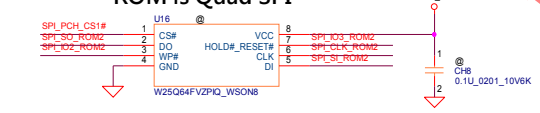
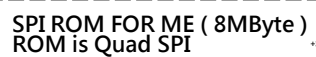
+3.3V_SPI

RH56 1 2 1K 0201 5% SPI_PCH_I02

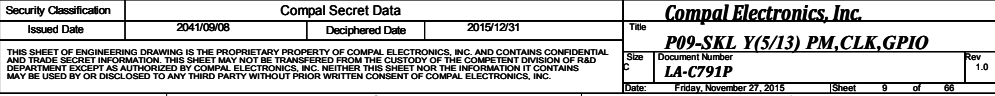
RH48 1 2 1K 0201 5% SPI_PCH_I03

RH49 1 2 1K 0201 5% SPI_PCH_I03

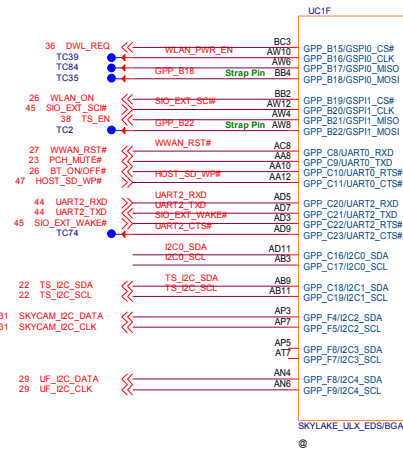
Intel's issue, For ES only
Refer MOW 2014WW36



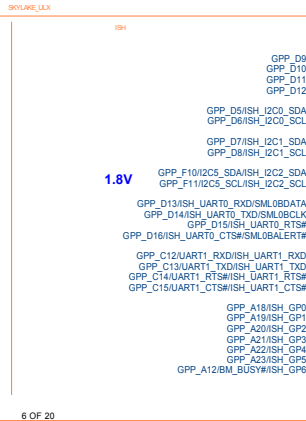
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2041/09/08	Deciphered Date	2015/12/31	Title	P07-SKL Y(3/13) SPL, SMBus, LPC	
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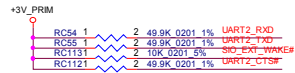
Codec, AMP
Touch Screen
Skycam PMIC
UF CAM



1.8V



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Functional Strap Definitions

GSPI0_MOSI / GPP_B18 (Internal Pull Down) :

No Reboot

0 = Disable No Reboot mode.

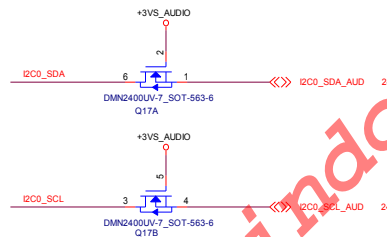
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI / GPP_B22 (Internal Pull Down) :

Boot BIOS Strap Bit

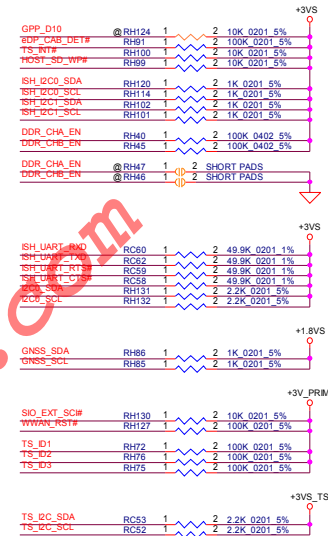
0 = SPI Mode

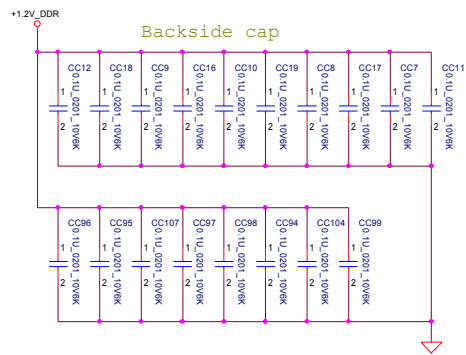
1 = LPC Mode



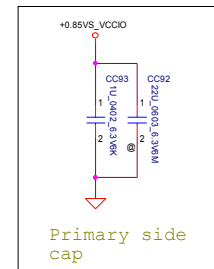
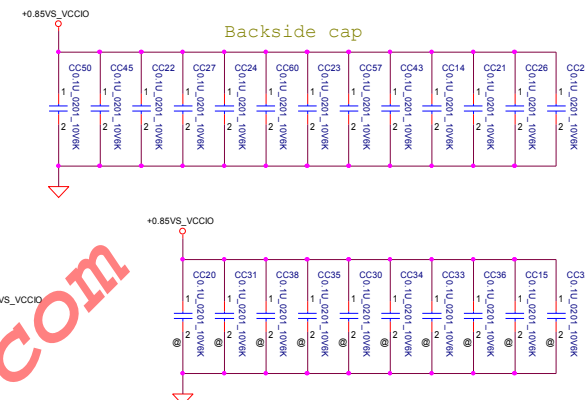
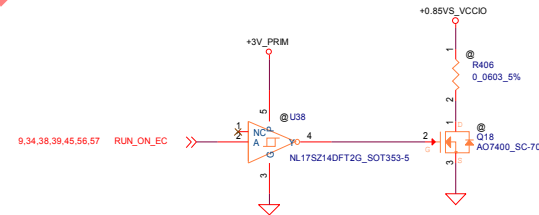
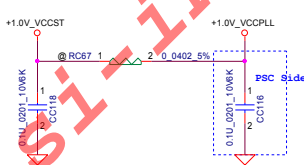
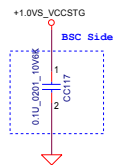
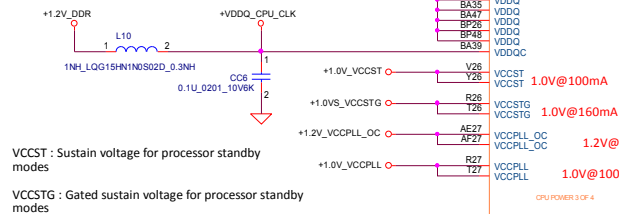
Sensors

WWAN GNSS

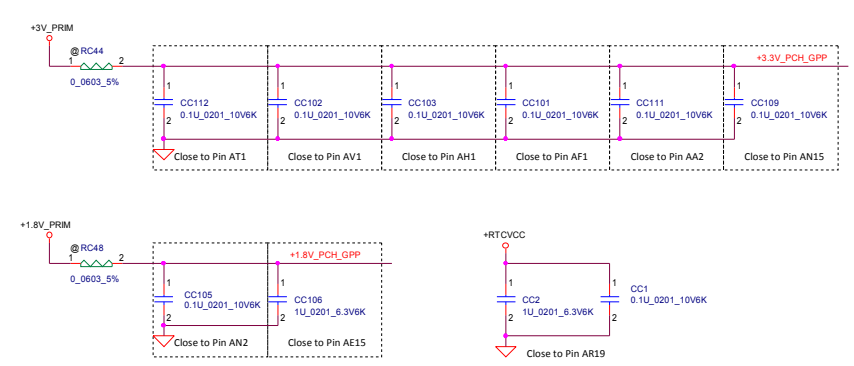
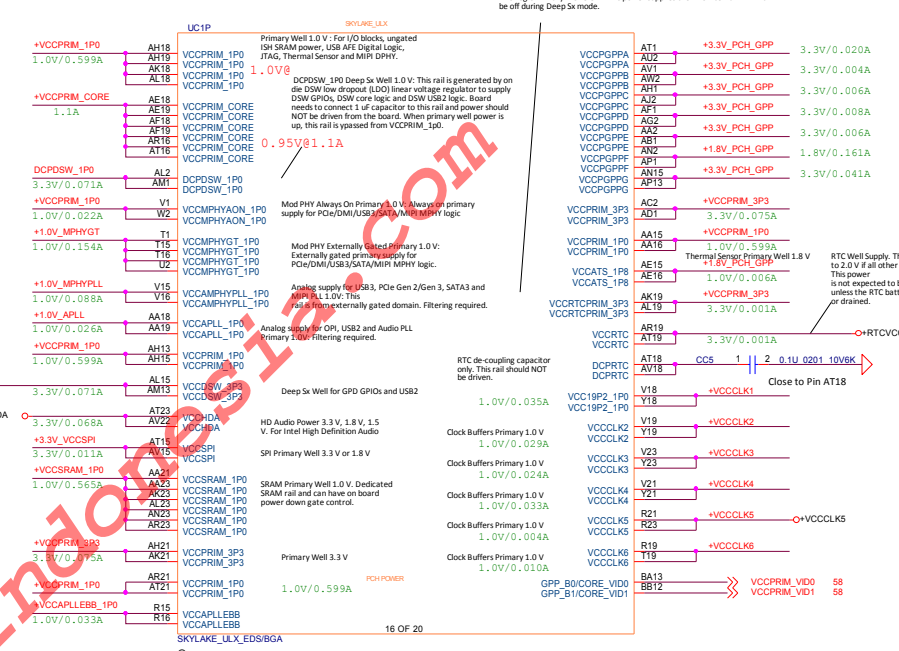




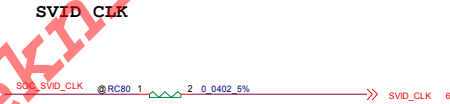
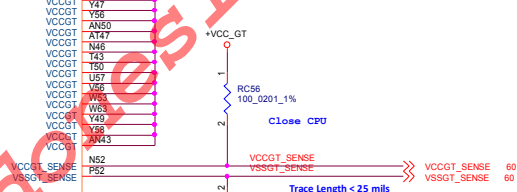
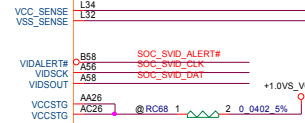
VDDQC trace
filter width = 6mm
Total etch length
= 186.94mils
PDG P597



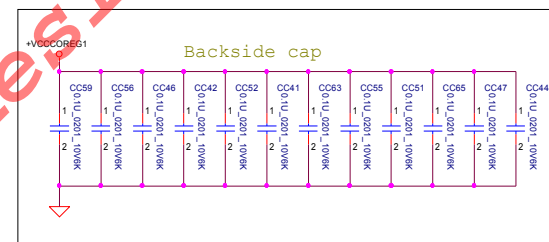
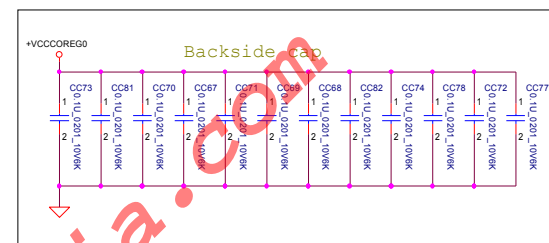
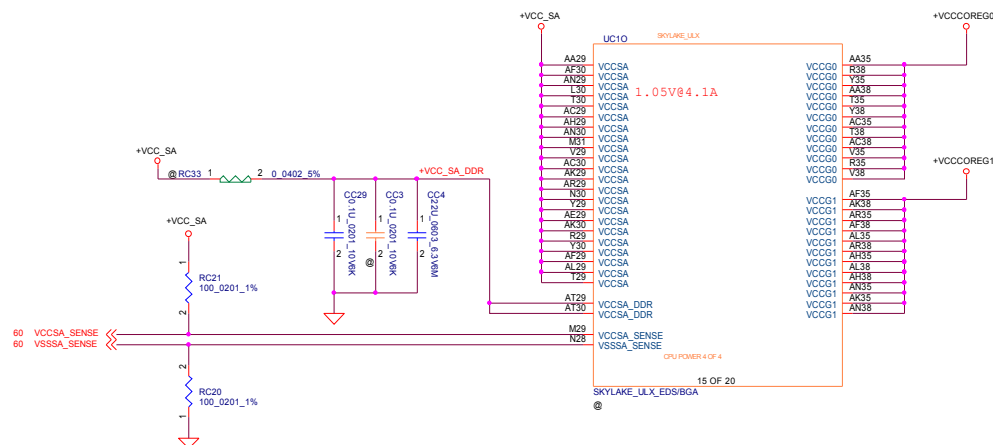
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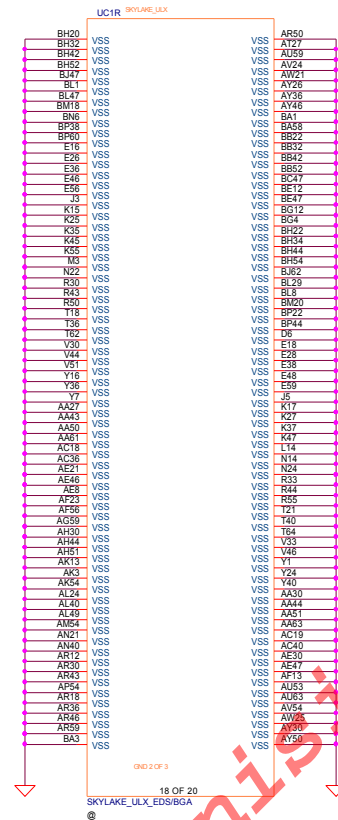
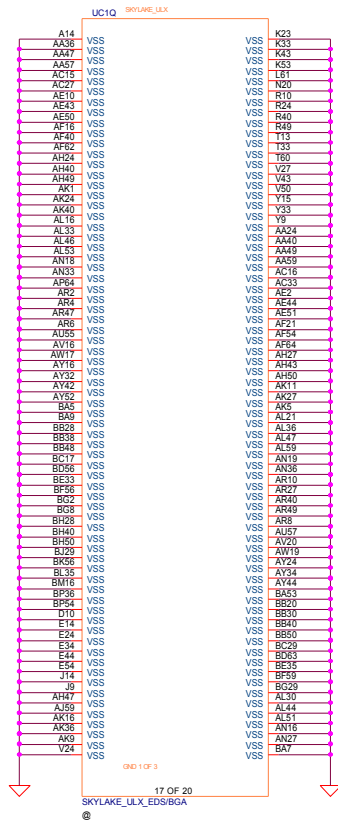


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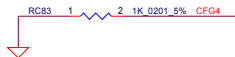


Functional Strap Definitions

CFG[4] : Display Port Presence strap

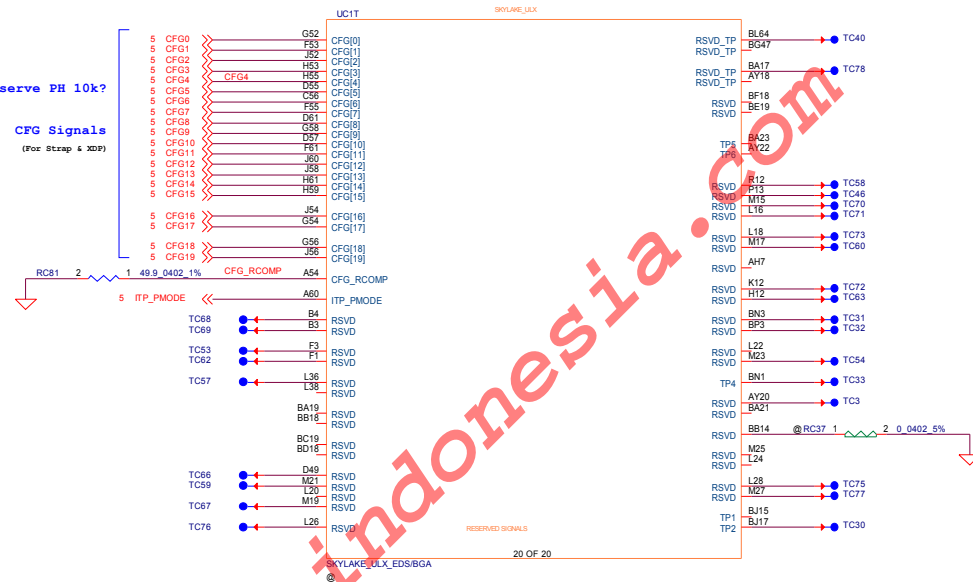
0 = Enabled - A Display Port device is connected to the Embedded Display Port.
No connect for disable.

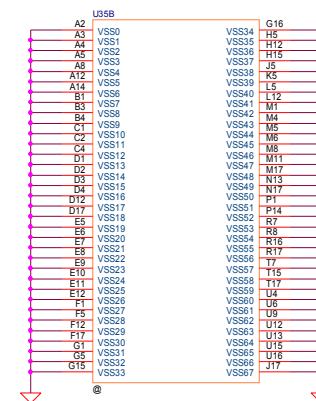
1 = Disabled - No Physical Display Port attached to Embedded DisplayPort*.
Pull-down to GND through a 1 K \pm 5% resistor to enable port.



CRB : Reserve PH 10k?

CFG Signals
(For Strap & XDP)



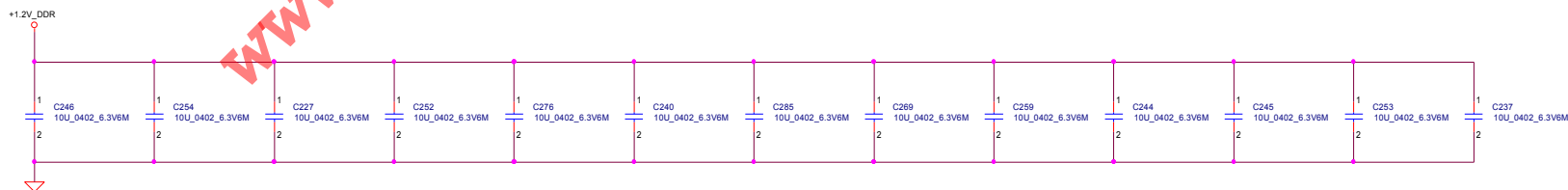
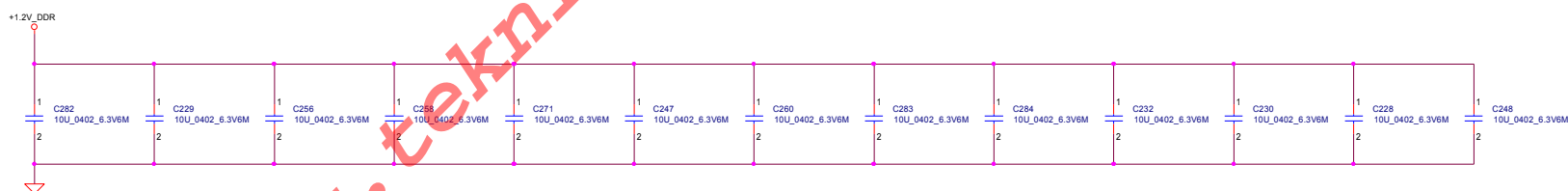
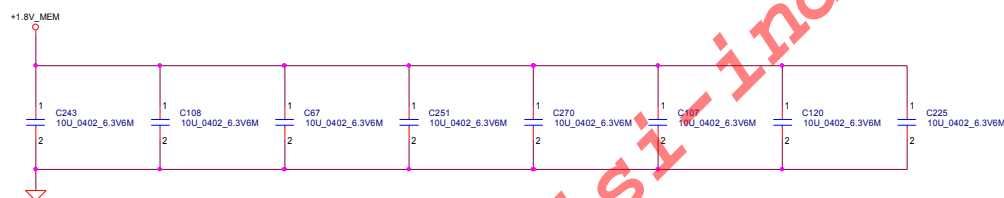
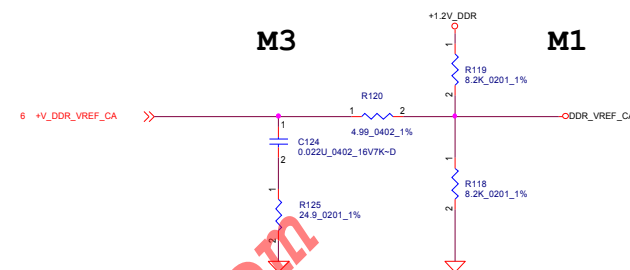
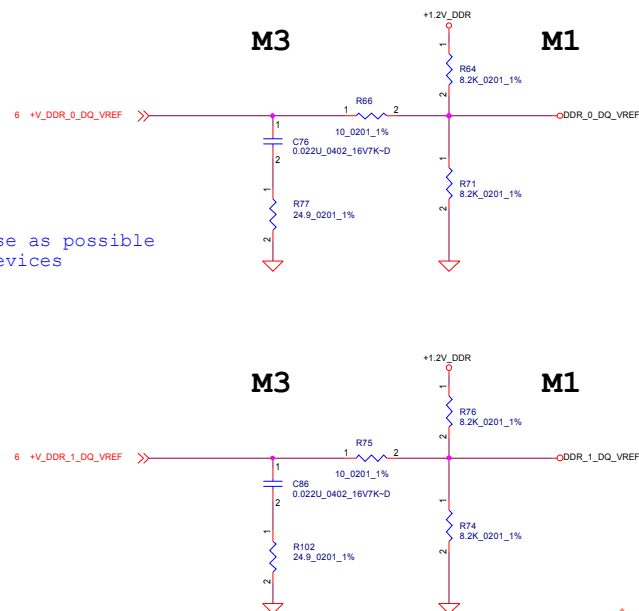


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					Size	Document Number	Rev	
					LA-C791P			1.0
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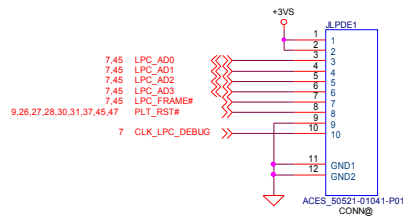
All VREF traces should
have 10 mil trace width

Place the VREF voltage divider as close as possible
to the LPDDR3 x64 memory down DREM devices

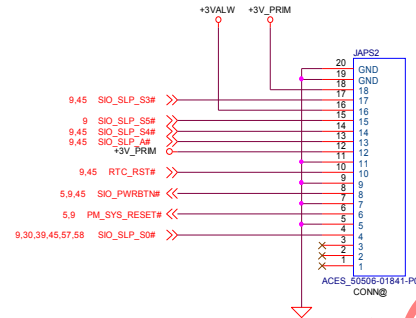


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BIOS debug



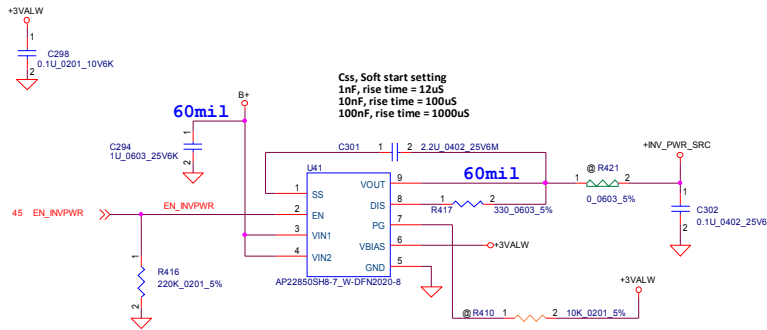
APS



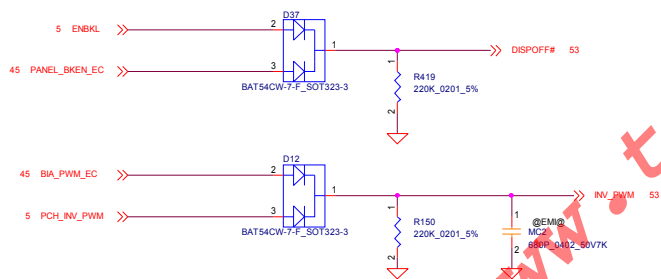
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		Deciphered Date		2013/10/28	
				P21-APS, Debug CONN	
				LA-C791P	
				Rev 1.0	
				Date: Friday, November 27, 2015	
				Sheet 21 of 66	

eDP BackLight Power

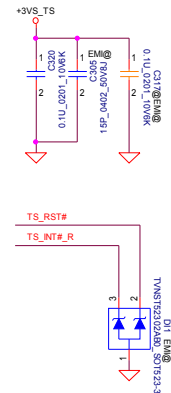
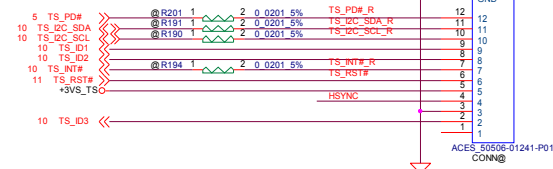
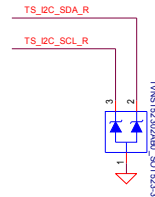
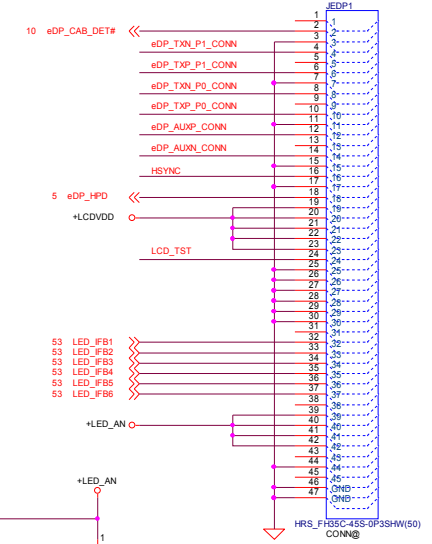
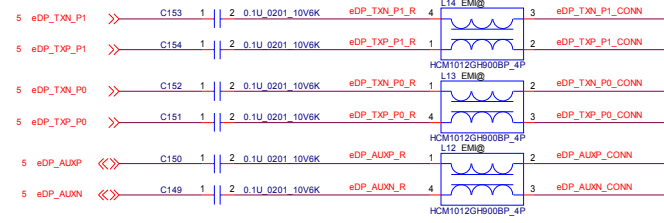


BackLight PWM Control



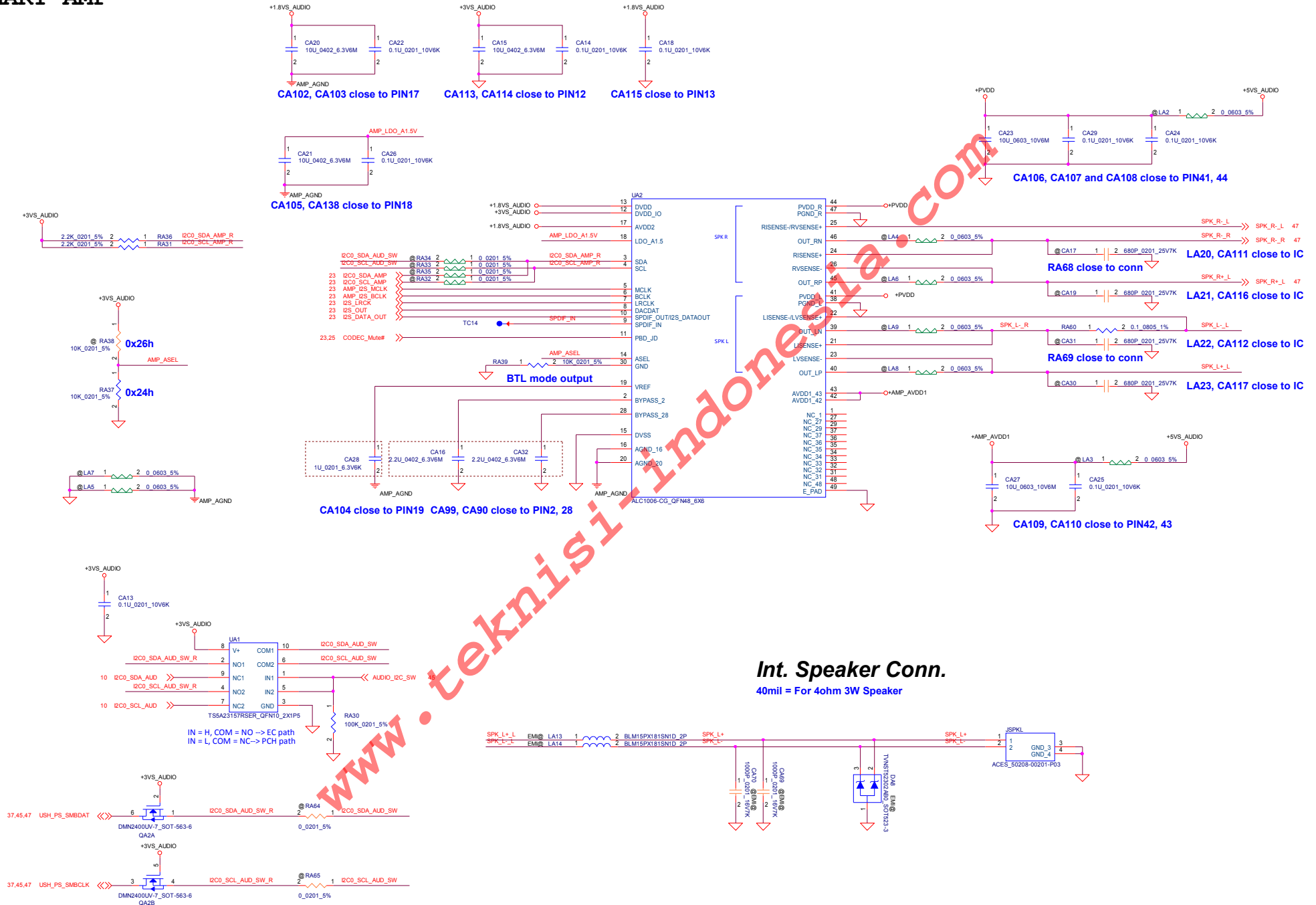
ITOUCH

eDP Conn



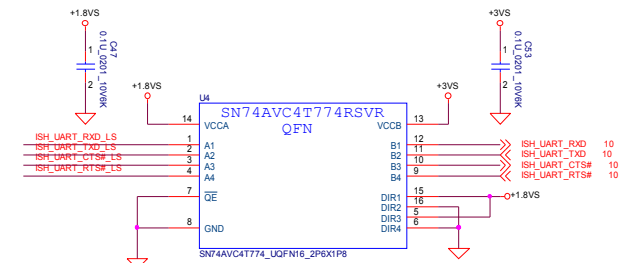
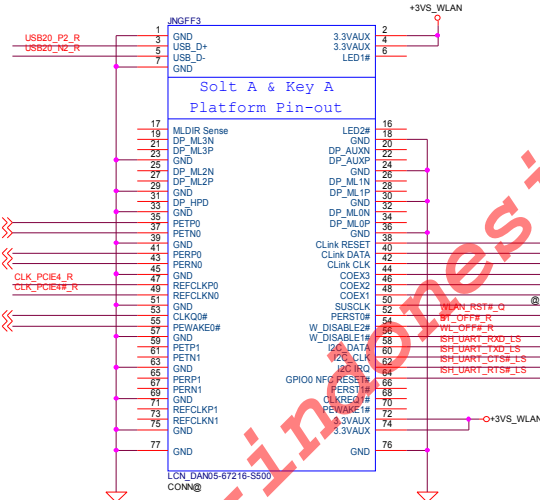
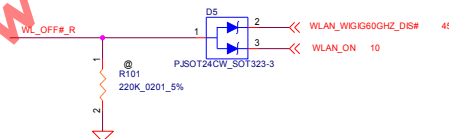
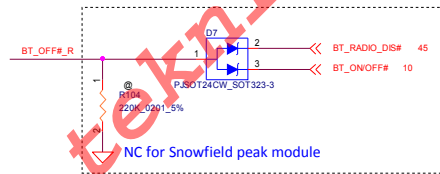
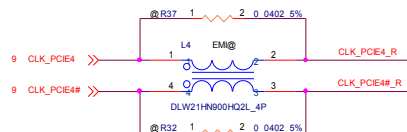
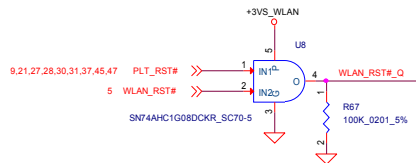
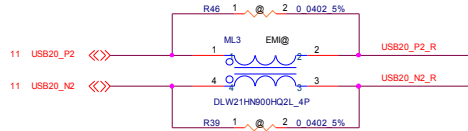
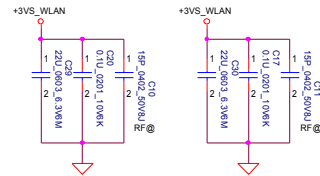
Security Classification	Compal Secret Data		Title	
Issued Date	2041/09/06	Deciphered Date	2013/10/28	P22-eDP, TS
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				1.0
				Date
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SMART AMP

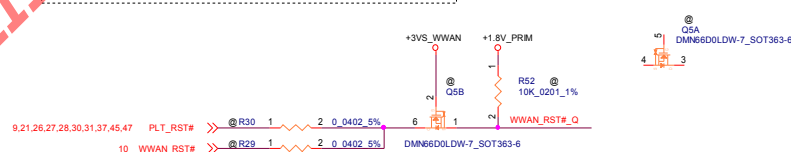
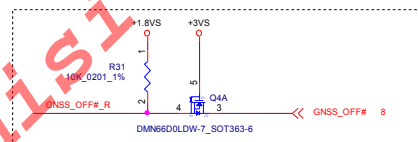
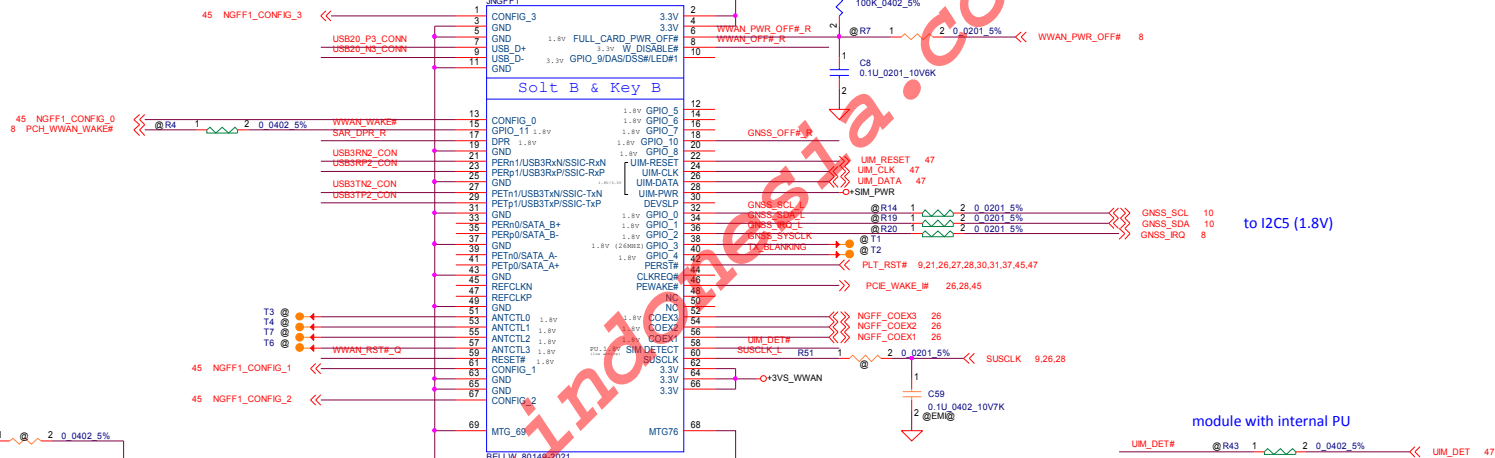
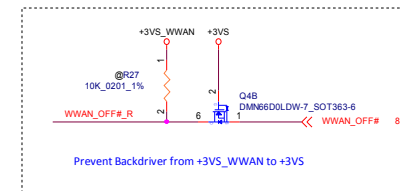


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2041/09/06	Deciphered Date	2013/10/28	Title	P24-Smart AMP/SPK CONN
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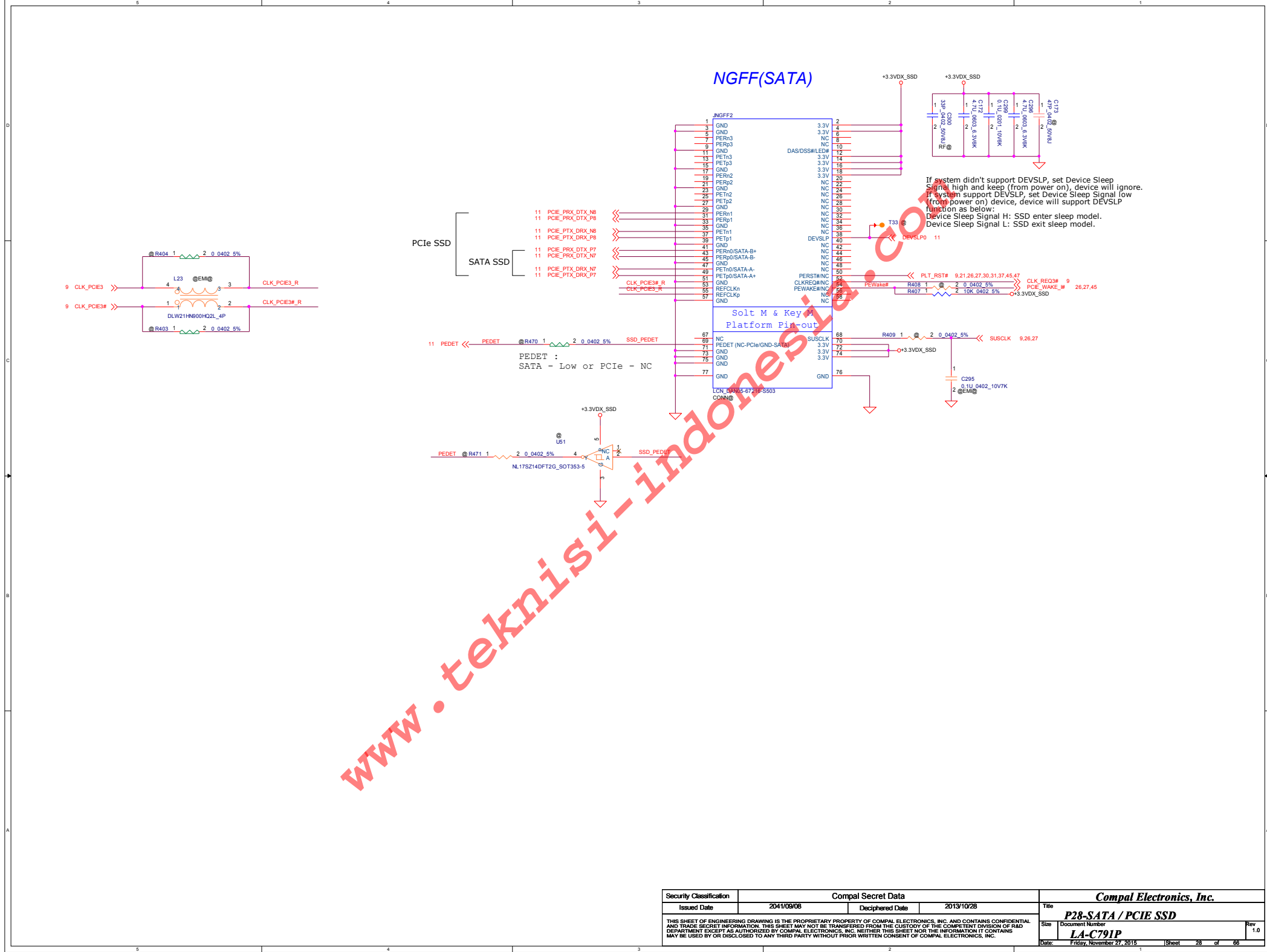
closed to pin 2, 4 closed to pin 64, 66

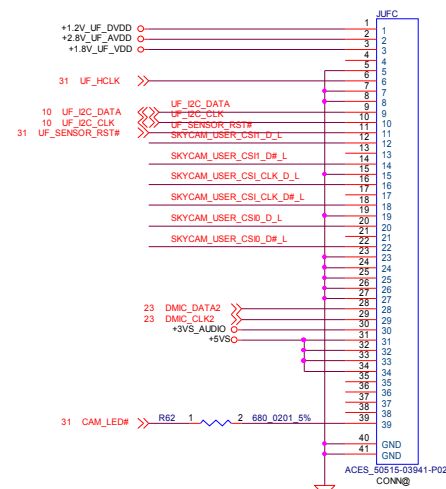
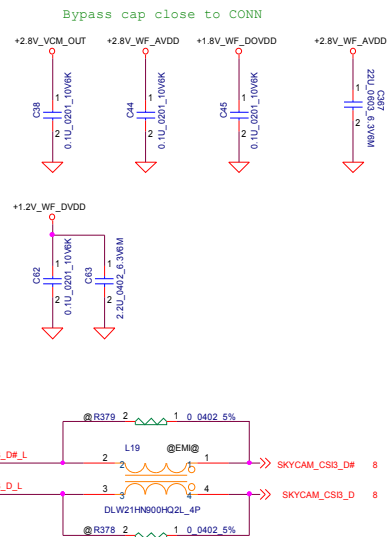


CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION	
OE	DIR	A PORT	B PORT		
L	L	Enabled	Hi-Z	B data to A data	
L	H	Hi-Z	Enabled	A data to B data	
H	X	Hi-Z	Hi-Z	Isolation	



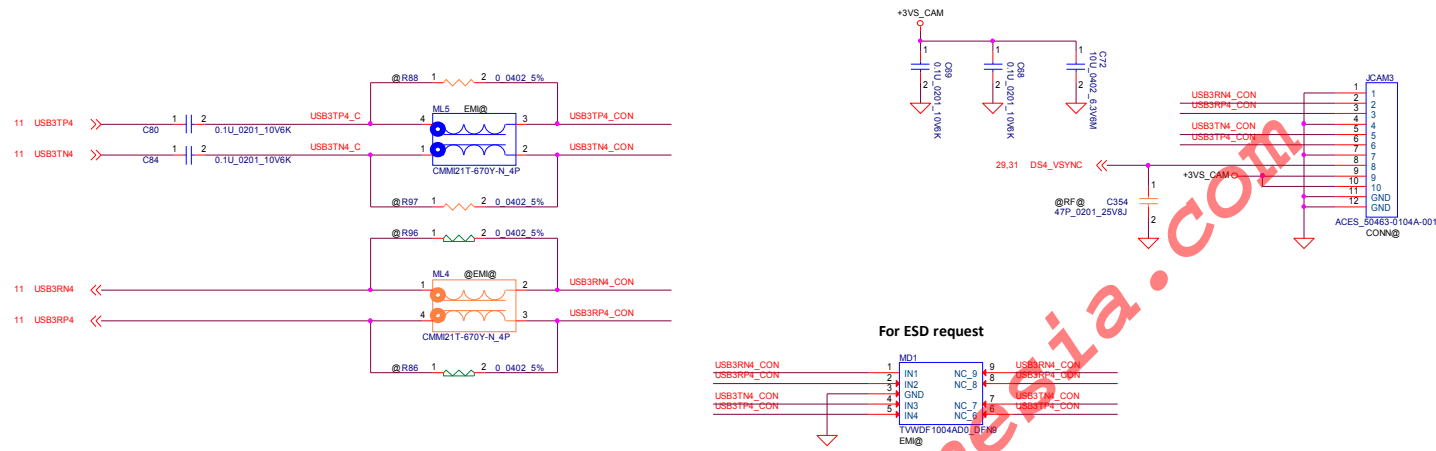
State#	CONFIG 0 (Pin 21)	CONFIG 1 (Pin 69)	CONFIG 2 (Pin 75)	CONFIG 3 (Pin 11)	Module Type	Port Configuration	Pin	Port Config_0	Port Config_1	Port Config_2	Port Config_3
0	GND	GND	GND	GND	SSD - SATA	N/A	GPIO_0	GNSS_SCL	GNSS_SCL	SIM_DET2	IPC_0
1	GND	HIGH	GND	GND	SSD - PCIe	N/A	GPIO_1	GNSS_SDA	GNSS_SDA	UIM_DTA2	IPC_1
2	GND	GND	HIGH	GND	WWAN - PCIe	0	GPIO_2	GNSS_IRQ	GNSS_IRQ	UIM_CLK2	IPC_2
3	GND	HIGH	HIGH	GND	WWAN - PCIe	1	GPIO_3	SYSCLK	GNSS_0	UIM_RST2	IPC_3
4	GND	GND	GND	HIGH	WWAN - USB 3.0	0	GPIO_4	TX BLANKING	GNSS_1	UIM_PWR2	IPC_4
5	GND	HIGH	GND	HIGH	WWAN - USB 3.0	1	GPIO_5	AUDIO_0	AUDIO_0	RFU	AUDIO_0
6	GND	GND	HIGH	HIGH	WWAN - USB 3.0	2	GPIO_6	AUDIO_1	AUDIO_1	RFU	AUDIO_1
7	GND	HIGH	HIGH	HIGH	WWAN - USB 3.0	3	GPIO_7	AUDIO_2	AUDIO_2	RFU	IPC_5/AUDIO_2
8	HIGH	GND	GND	GND	WWAN - USB 3.0	2	GPIO_8	AUDIO_3	AUDIO_3	RFU	IPC_6/AUDIO_3
9	HIGH	HIGH	GND	GND	WWAN - SSIC	1	GPIO_9	LED 1#	LED 1#	LED 1#	IPC_7
10	HIGH	GND	HIGH	GND	WWAN - SSIC	2	GPIO_10	W_DISABLE2#	W_DISABLE2#	W_DISABLE2#	HSIC_STROBE
11	HIGH	HIGH	HIGH	GND	WWAN - SSIC	3	GPIO_11	WAKE_ON_WWAN#	WAKE_ON_WWAN#	WAKE_ON_WWAN#	HSIC_DATA
12	HIGH	GND	GND	HIGH	WWAN - PCIe	2					
13	HIGH	HIGH	GND	HIGH	WWAN - PCIe	3					
14	HIGH	GND	HIGH	HIGH	DDP/HCA - PCIe	N/A					
15	HIGH	HIGH	HIGH	HIGH	No Module	N/A					



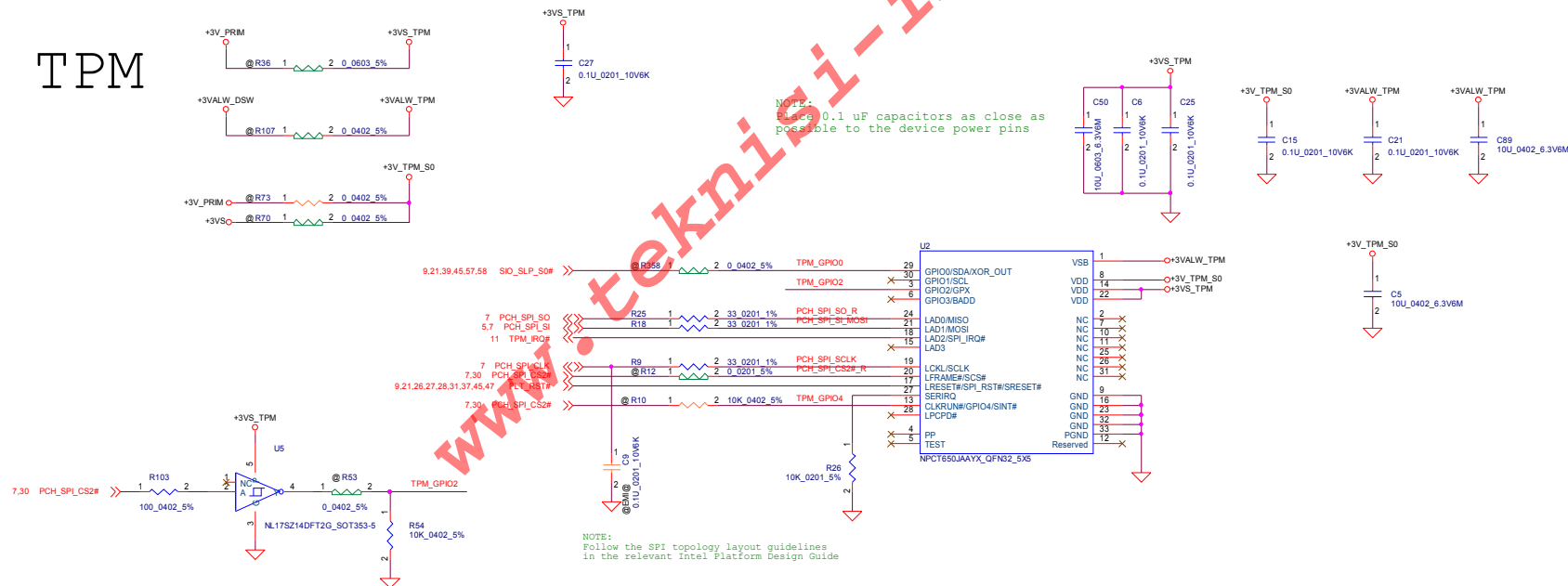


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				Size	Document Number
				LA-C791P	
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				Sheet 29 of 66	

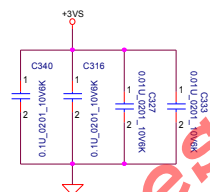
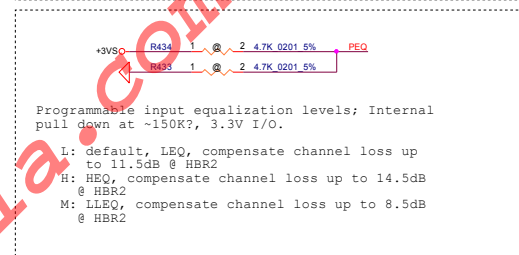
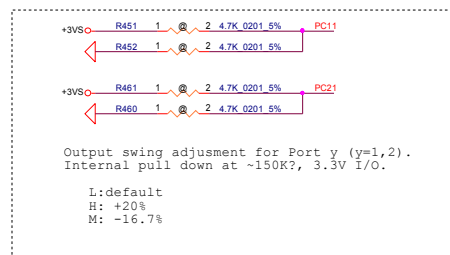
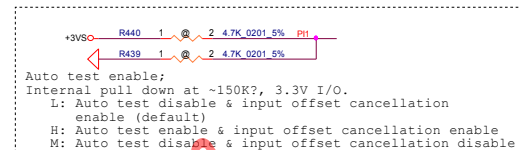
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TPM



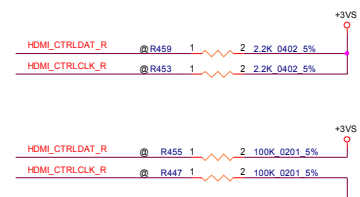
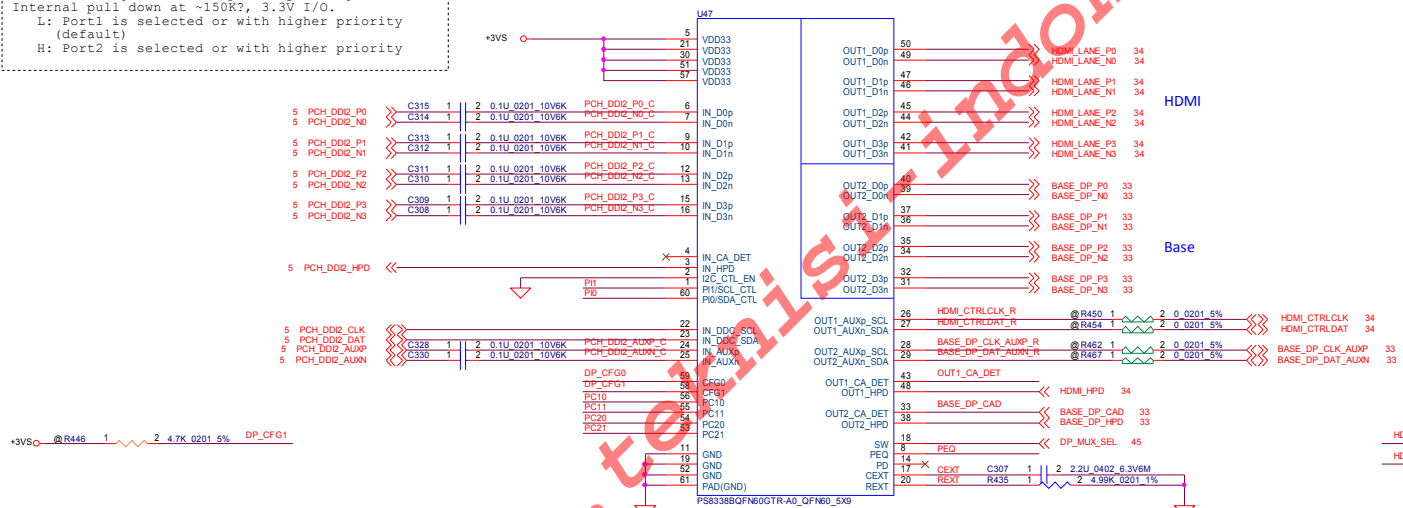
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Issued Date	2041/09/06	Deciphered Date	2013/10/28	Title	P30-DS4 Camera / TPM
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Port switching control or priority configuration;
Internal pull down at ~150K $\Omega$ , 3.3V I/O.
  L: Port1 is selected or with higher priority
    (default)
  H: Port2 is selected or with higher priority

```



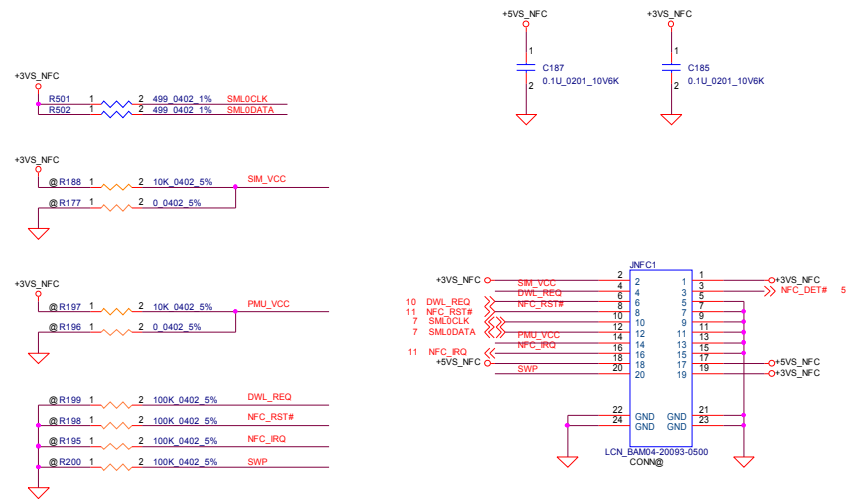
AUX N need Pull UP !! to enable internal AUX CH



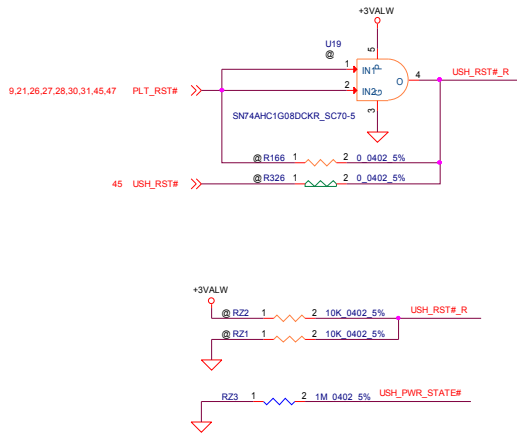
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						Size	Document Number		Rev
						LA-C791P			1.0
Date:		Friday, November 27, 2015		Sheet	32 of 66				



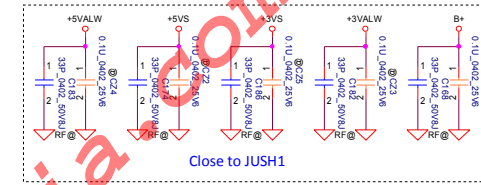
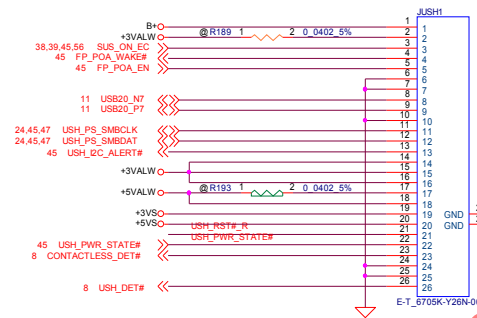
www.teknisi-indonesia.com



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Issued Date	2041/09/08	Deciphered Date	2013/10/28	Title	P36-NFC/Iris Scan
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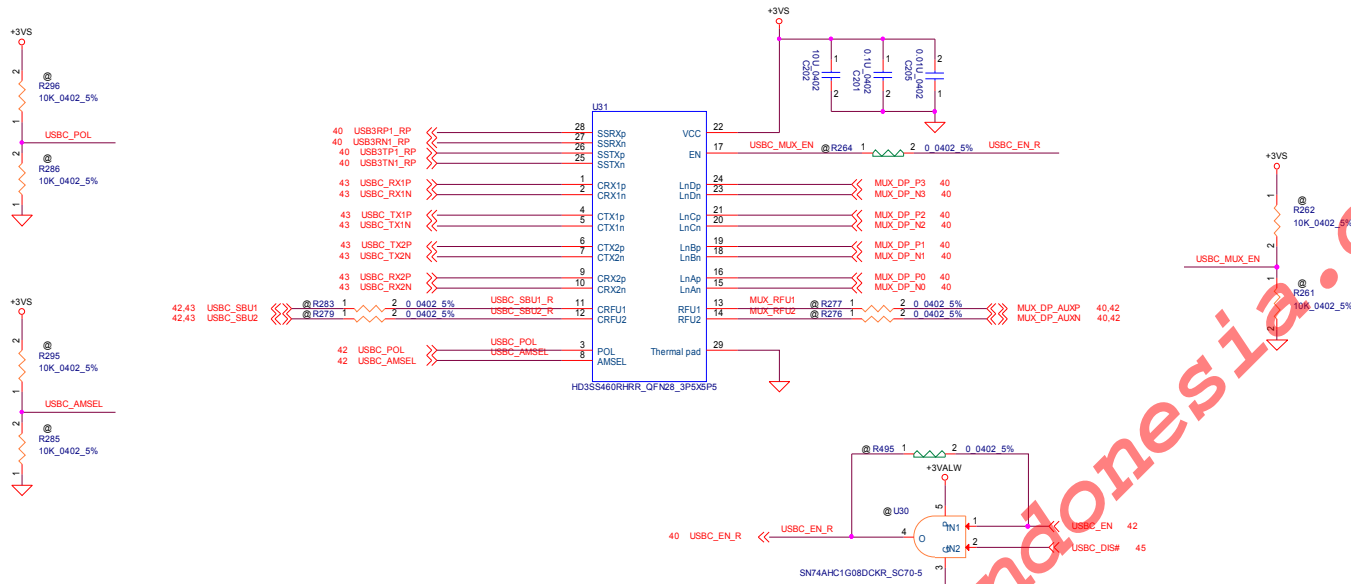
USH CONN



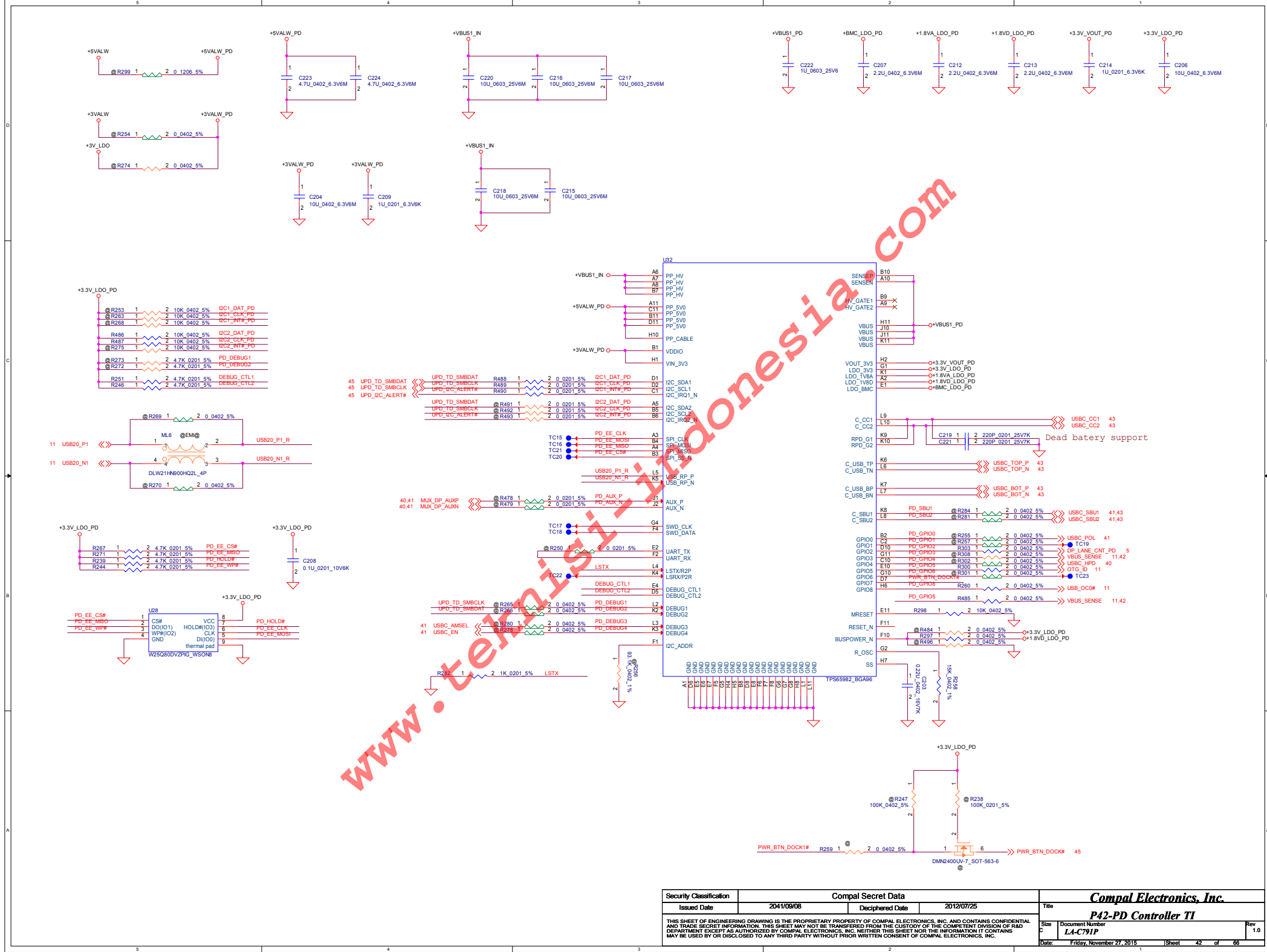
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Issued Date		Deciphered Date		Title	
2011/05/02		2013/10/28		P37-USH CONN	
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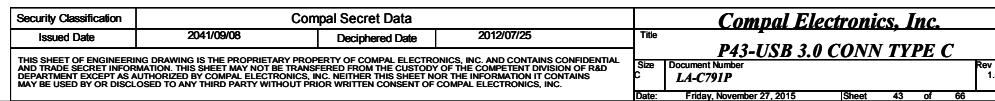
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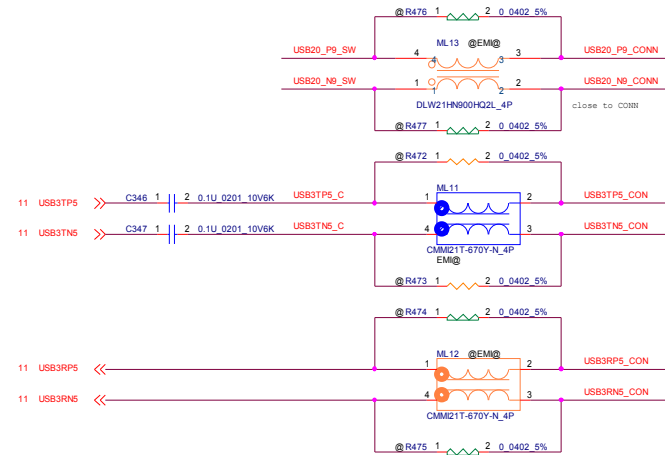


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size		Document Number		LA-C322P	
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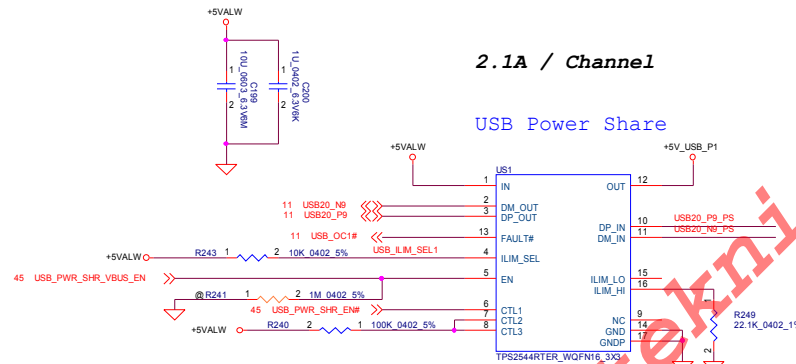
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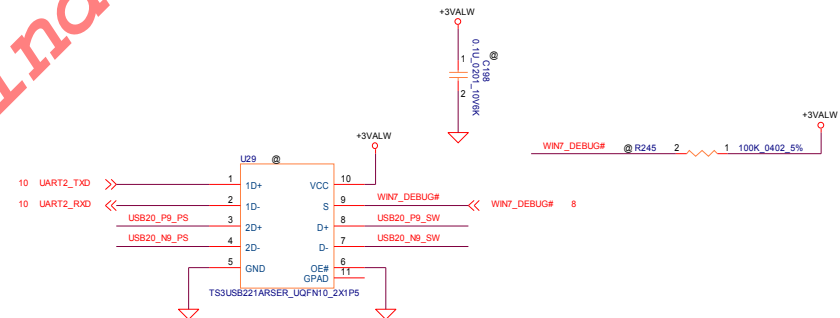
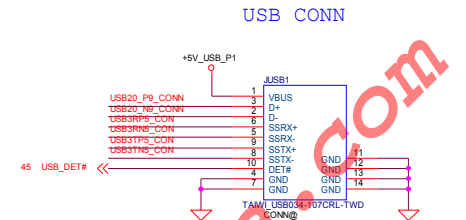


2.1A / Channel

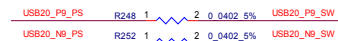
USB Power Share

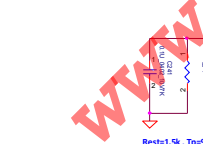
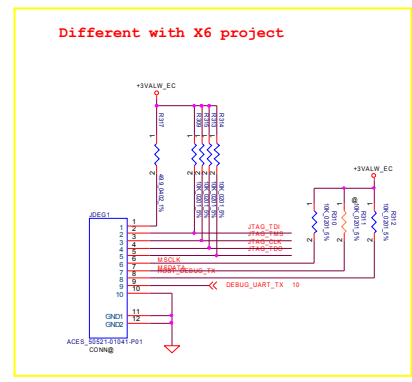
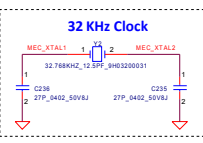
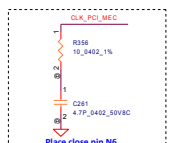
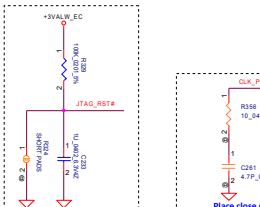
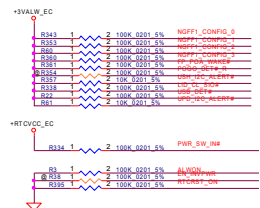
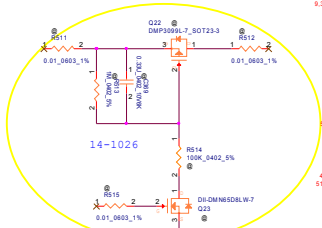
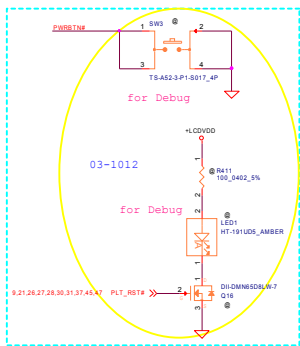


CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP Auto
0	1	1	1	DCP Auto
1	1	1	0	SDP
1	1	1	1	CDP

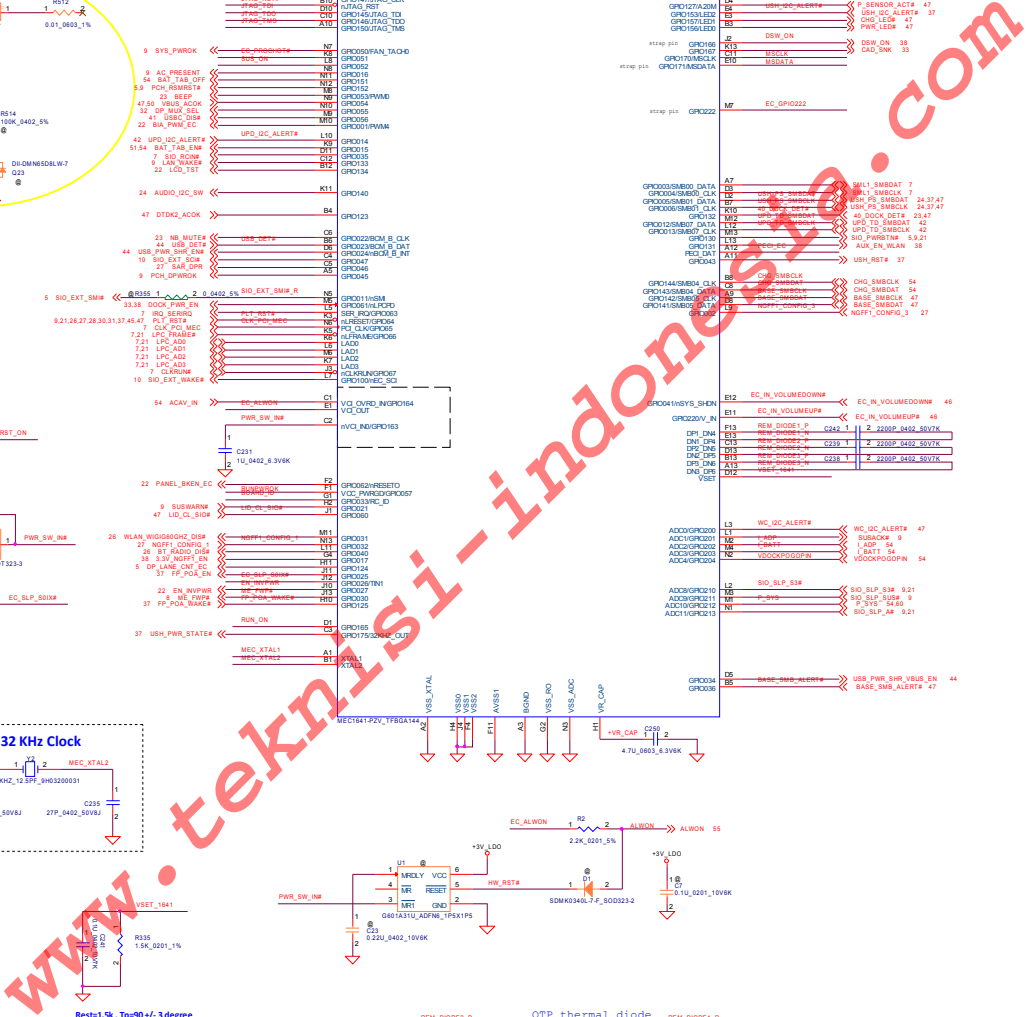
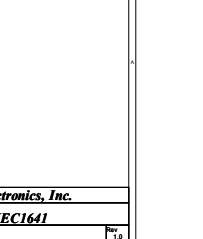
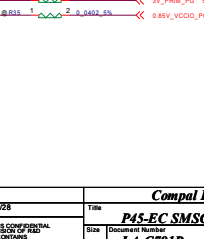
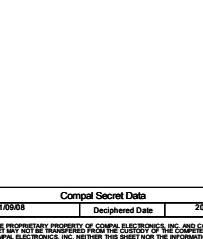
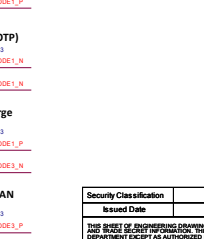
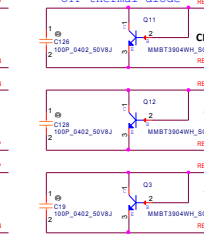
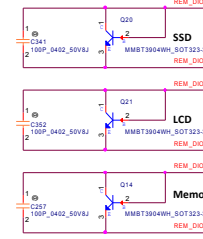


TRUTH TABLE
S OE FUNCTION
X H Disconnect
L L D = 1D
H L D = 2D

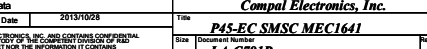
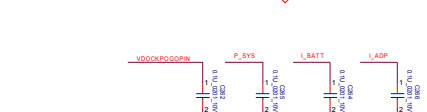
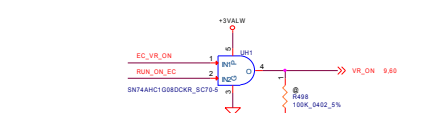
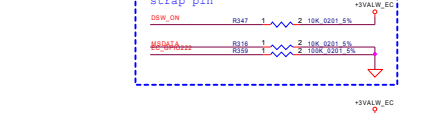
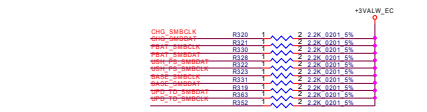




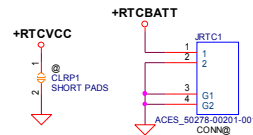
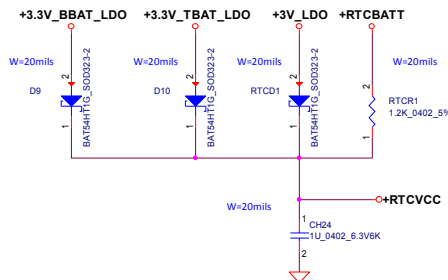
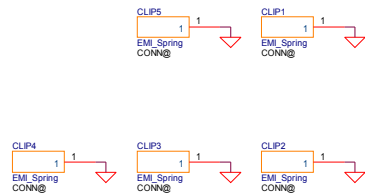
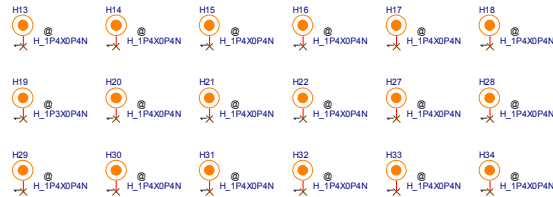
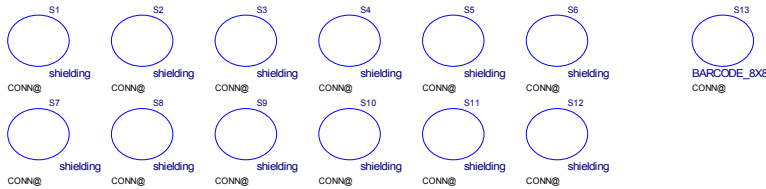
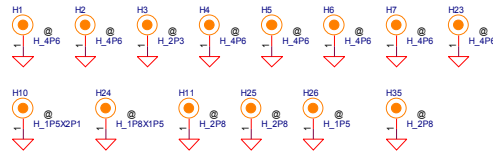
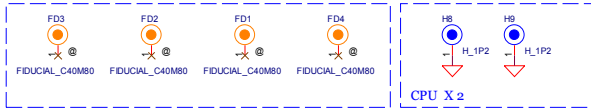
Thermal diode mapping	
DP1/DN1	CPU(OTP)
DP2/DN2	SSD
DP3/DN3	Memory
DP4/DN4	Charge
DP5/DN5	LCD
DP6/DN6	WWAN



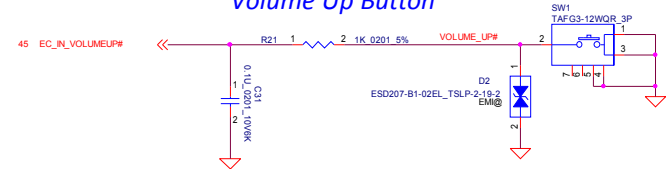
R	C	REV
240K	4700P	EVT1
130K	4700P	DVT1
62K	4700P	DVT2
33K	4700P	DVT3
8.2K	4700P	DVT3.1
4.3K	4700P	PVT
2K	4700P	
1K	4700P	



Screw Hole

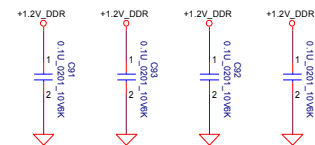
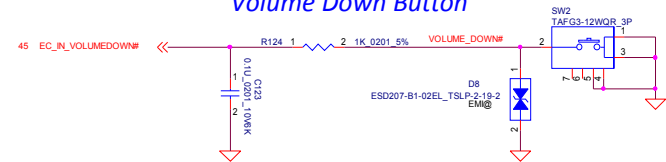


Volume Up Button

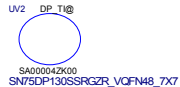
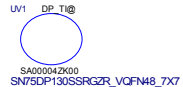
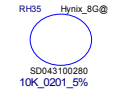
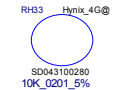
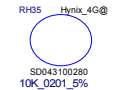
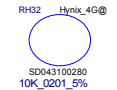
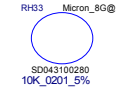
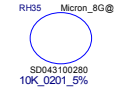
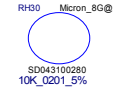
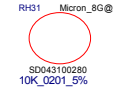
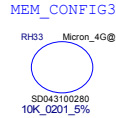
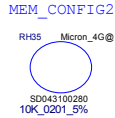
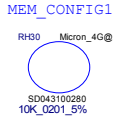
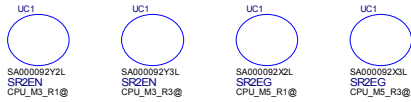


PU 10K resistor locate on EC side

Volume Down Button



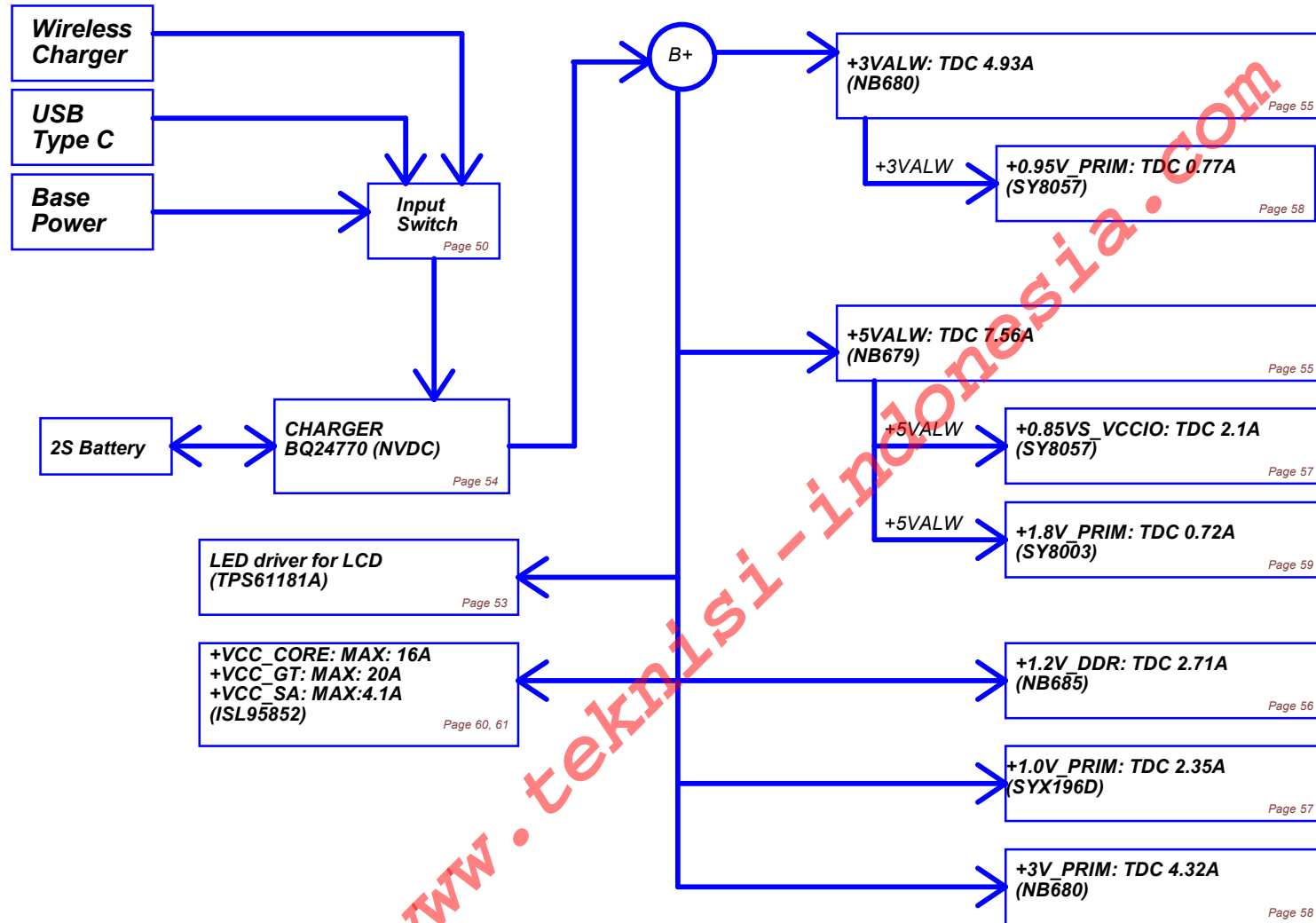
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2041/09/08	Deciphered Date	2013/10/28	Title	P46-RTC, VOL SW, SCREWH
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Date: Friday, November 27, 2015					Sheet 46 of 66



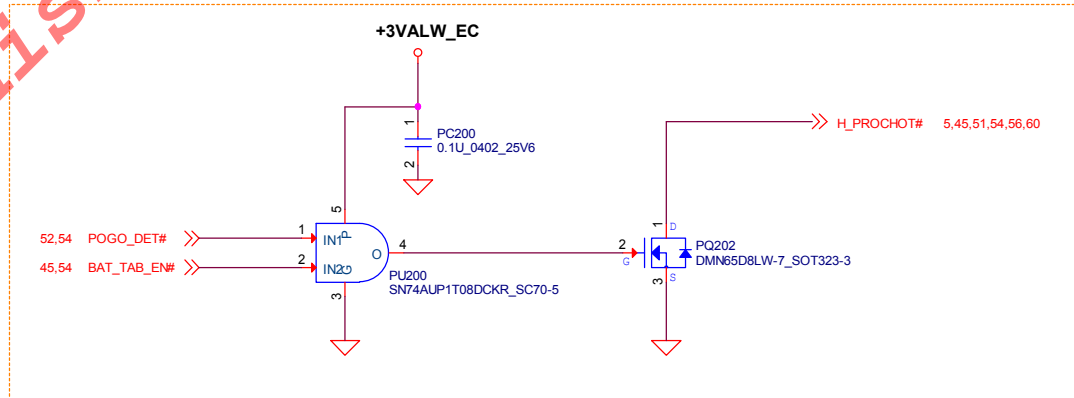
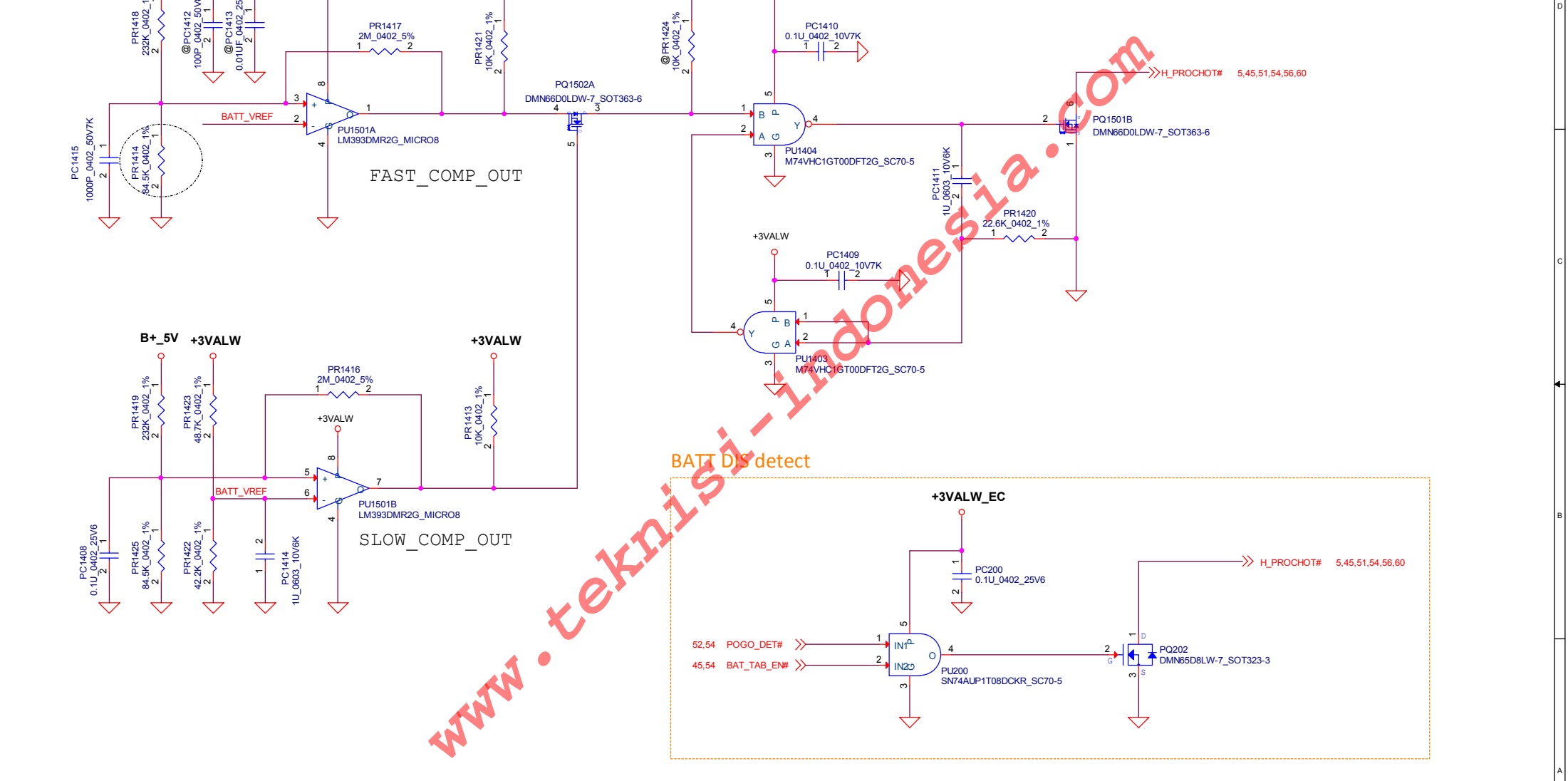
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2011/05/02		Title	
		Deciphered Date		2013/10/28	
				P48-BOM	
				Document Number	
				LA-C791P	
				Date: Friday, November 27, 2015	
				Sheet 48 of 66	
				Rev 1.0	

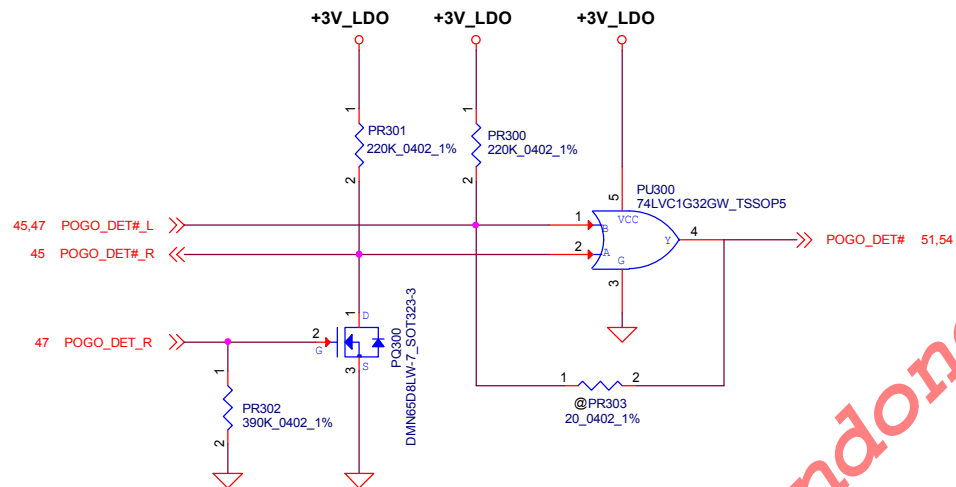
Jayton2 Power Block_Tablet



5	4	3	2	1
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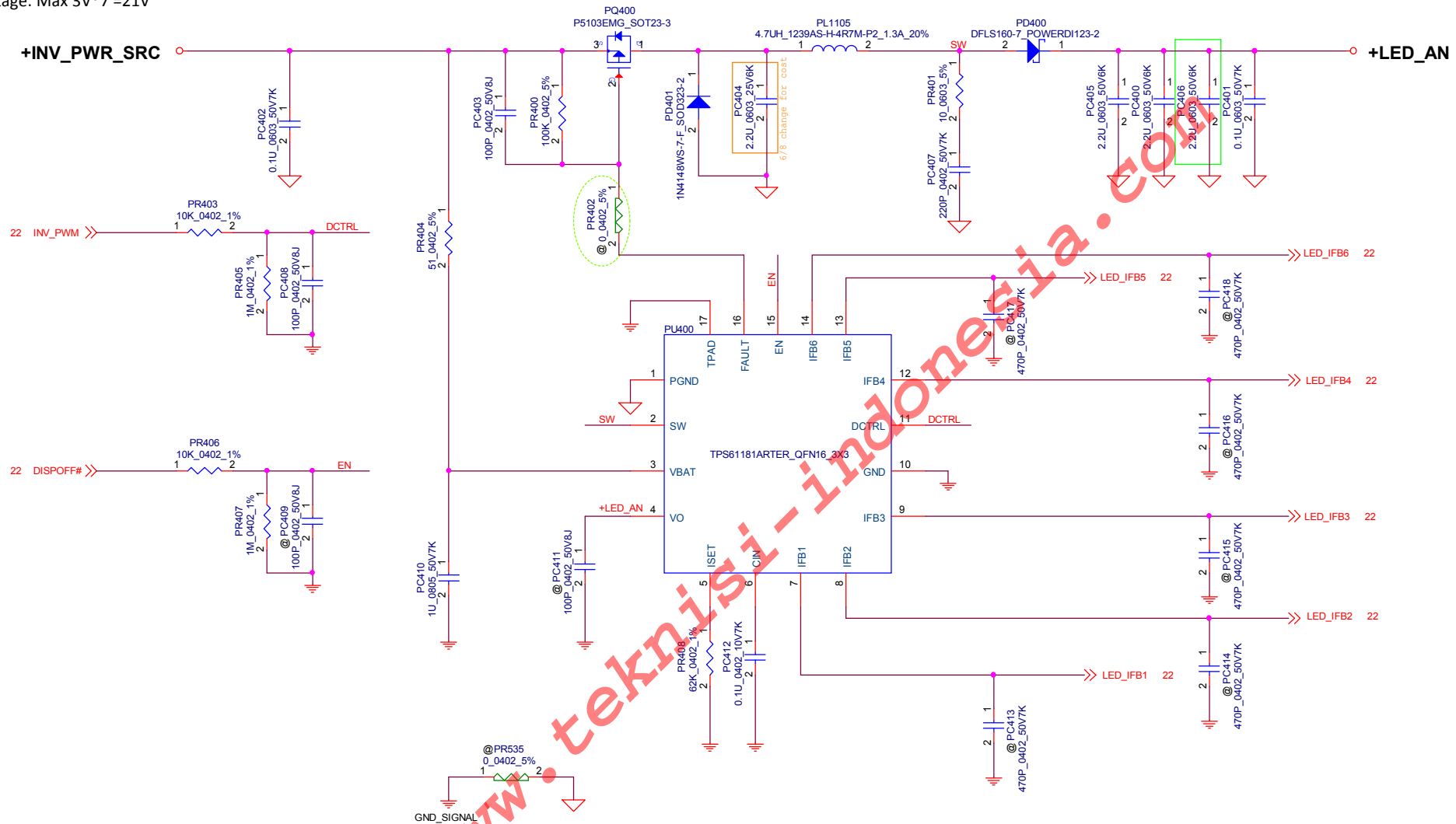
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	<u>PWR DIS BAT PROCHOT#</u>	
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				<Doc>		
Date:	Friday, November 27, 2015		Sheet	51	of	66



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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	PWR POGO_DET#
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				Date:	Friday, November 27, 2015
				Sheet	52 of 66

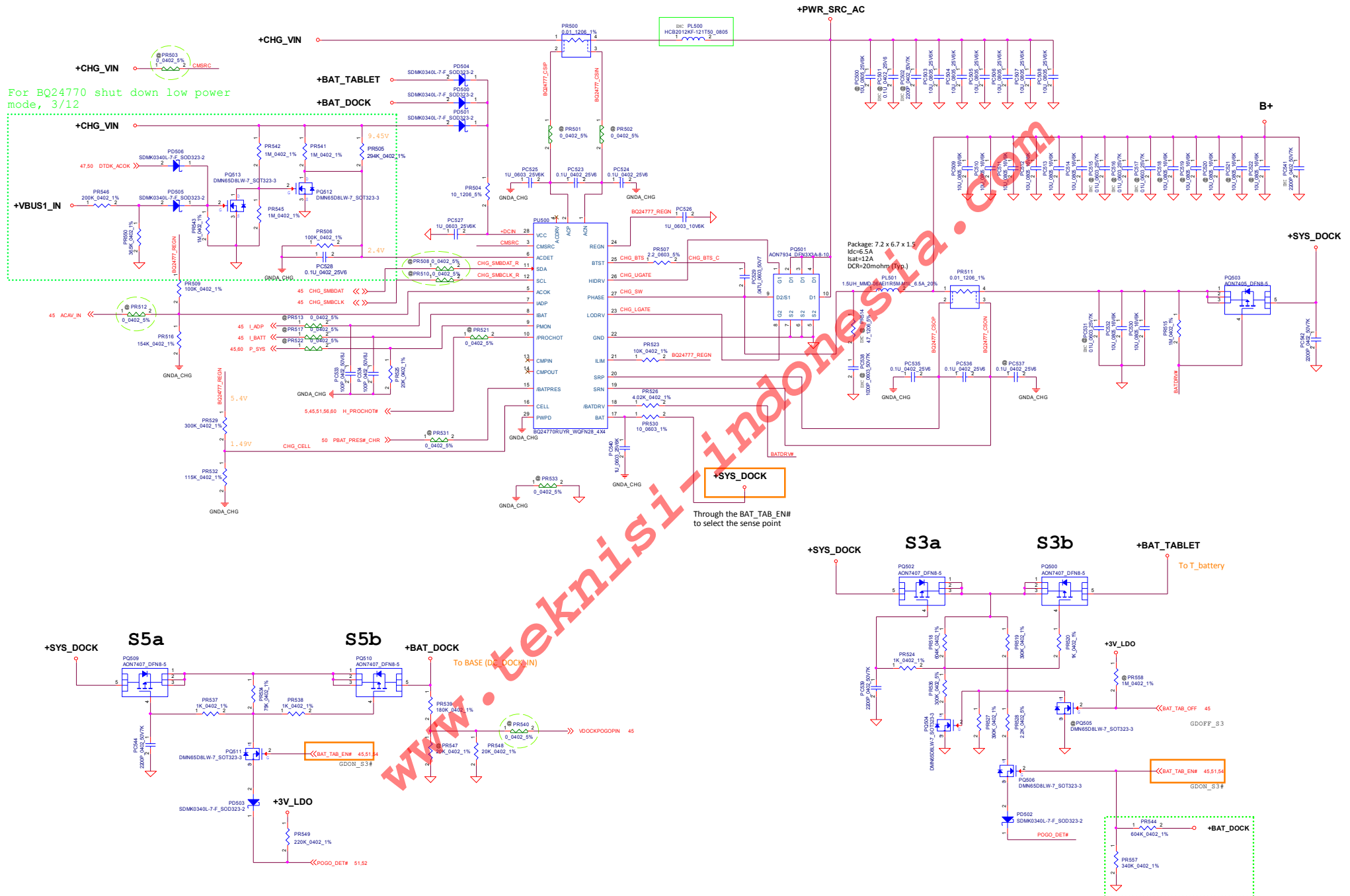
Current: Typ 19.5mA* 6= 117mA
Voltage: Max 3V*7 =21V



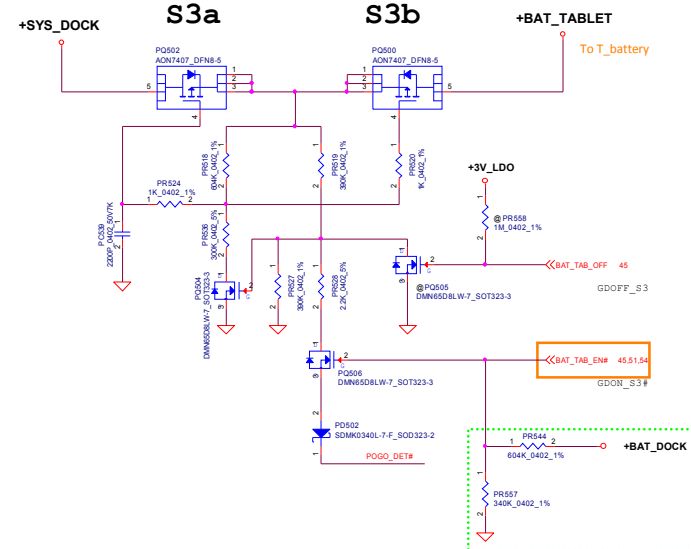
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	PWR LCD driver (TPS61181A)
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				Date:	Friday, November 27, 2015
				Sheet	53 of 66

Charger controller(40.1), Support component(40.2)

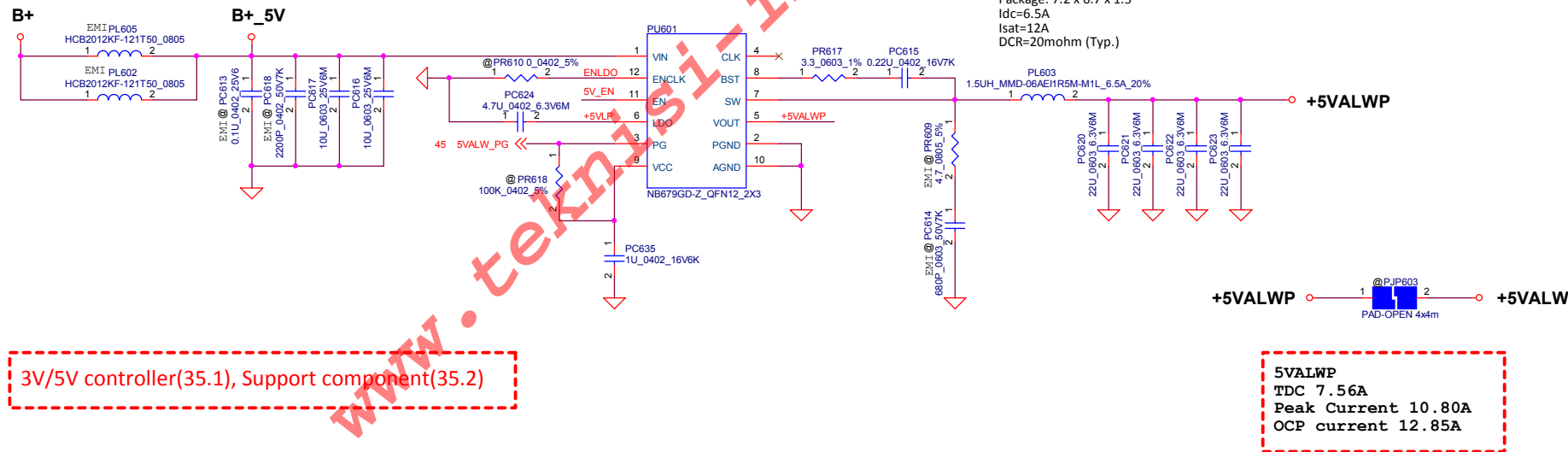
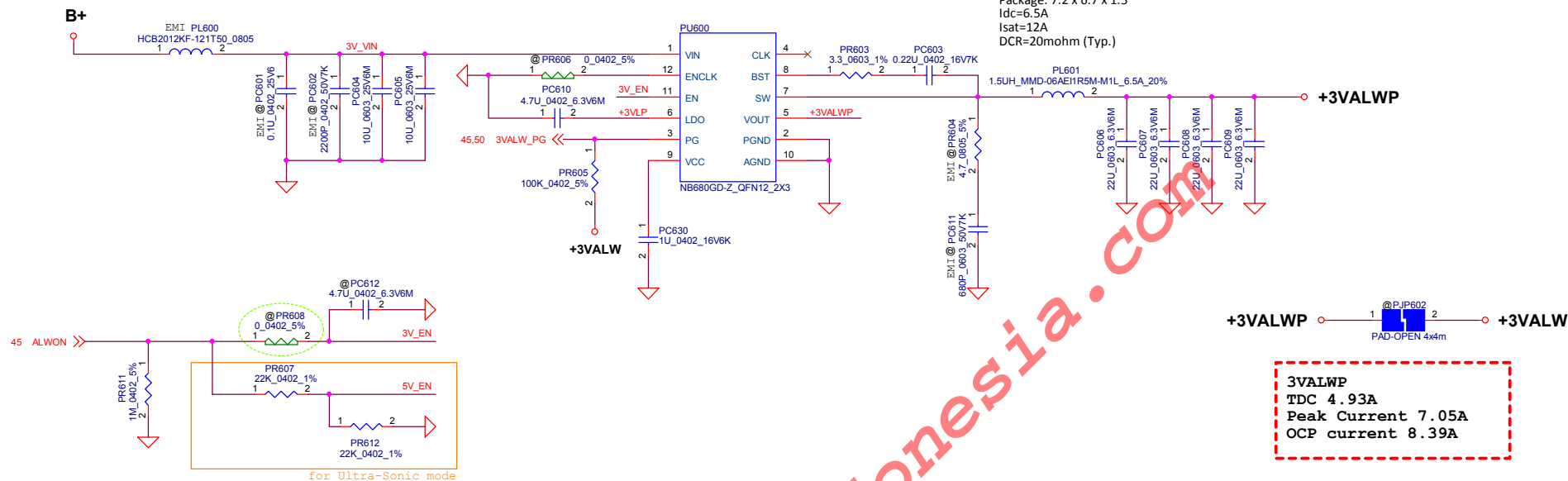
For BQ24770 shut down low power mode, 3/12



Through the BAT_TAB_EN# to select the sense point

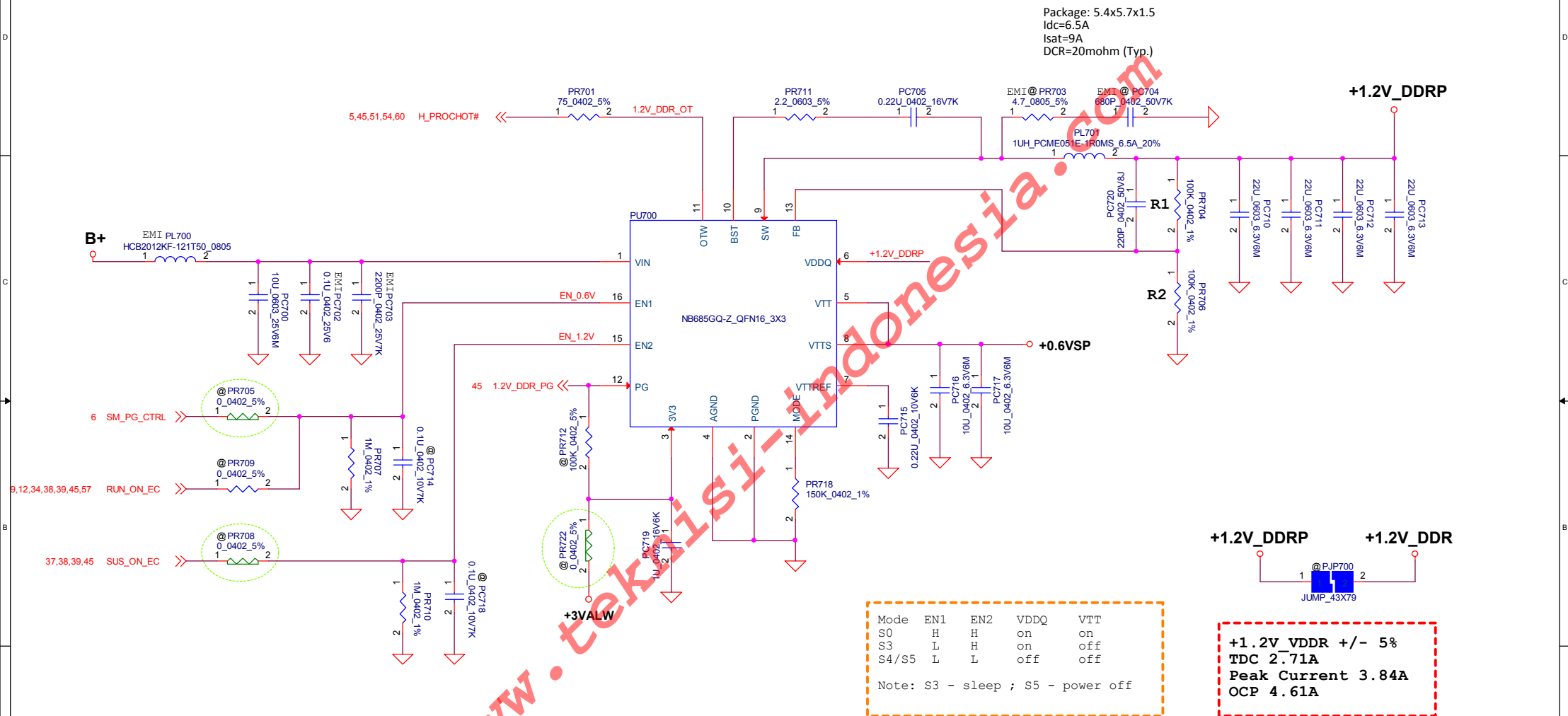


Security Classification			Compal Secret Data		Title	
Issued Date	2011/06/02	Deciphered Date	2013/10/26		Rev	1.0
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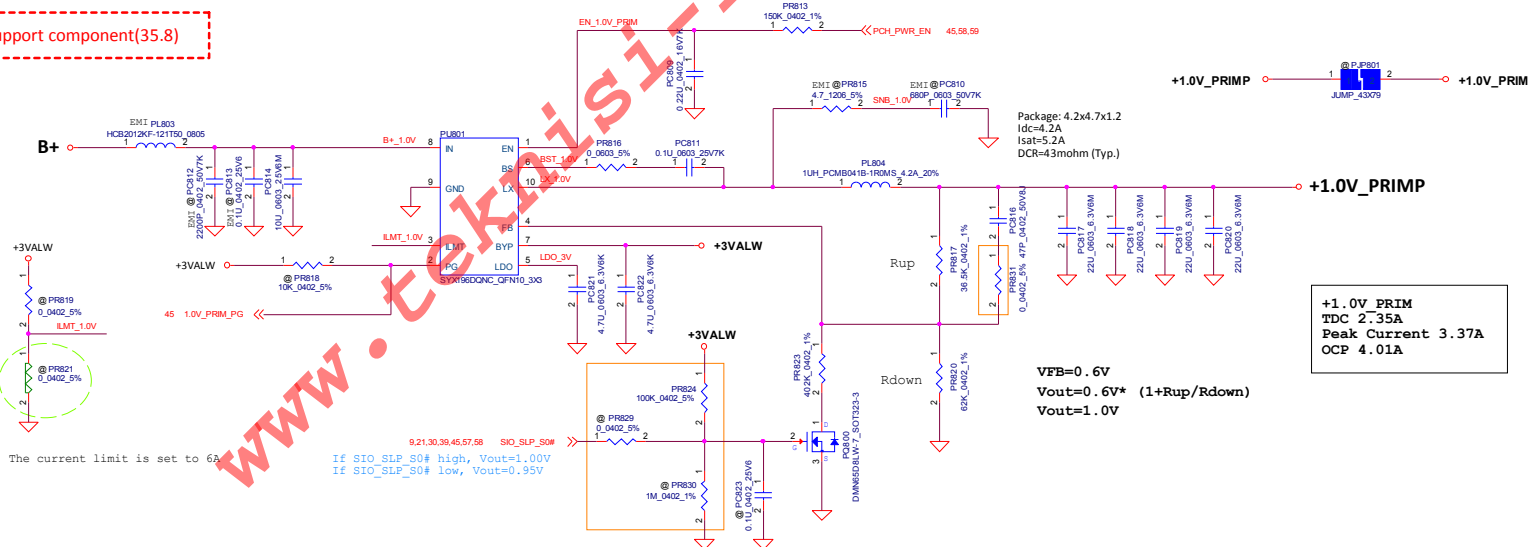
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	PWR +3V(NB680)/+5V(NB679)
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 1.0
				Date:	Friday, November 27, 2015
				Sheet	55 of 66

DDR controller(35.3), Support component(35.4)



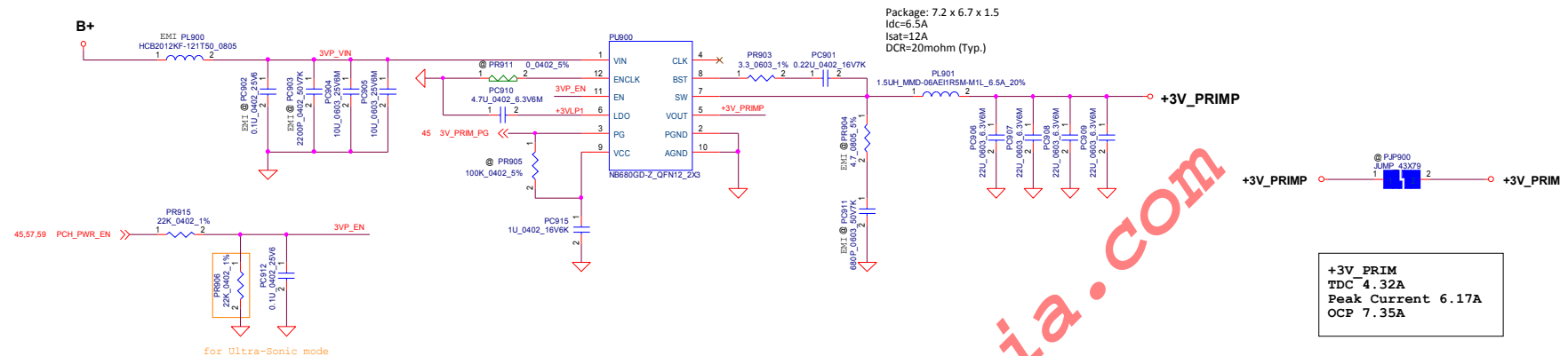
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/04/10	Deciphered Date	2014/05/01	Title	PWR +1.2V DDR(NB685)
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 1.0
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+1.0V PRIM controller(35.7), Support component(35.8)

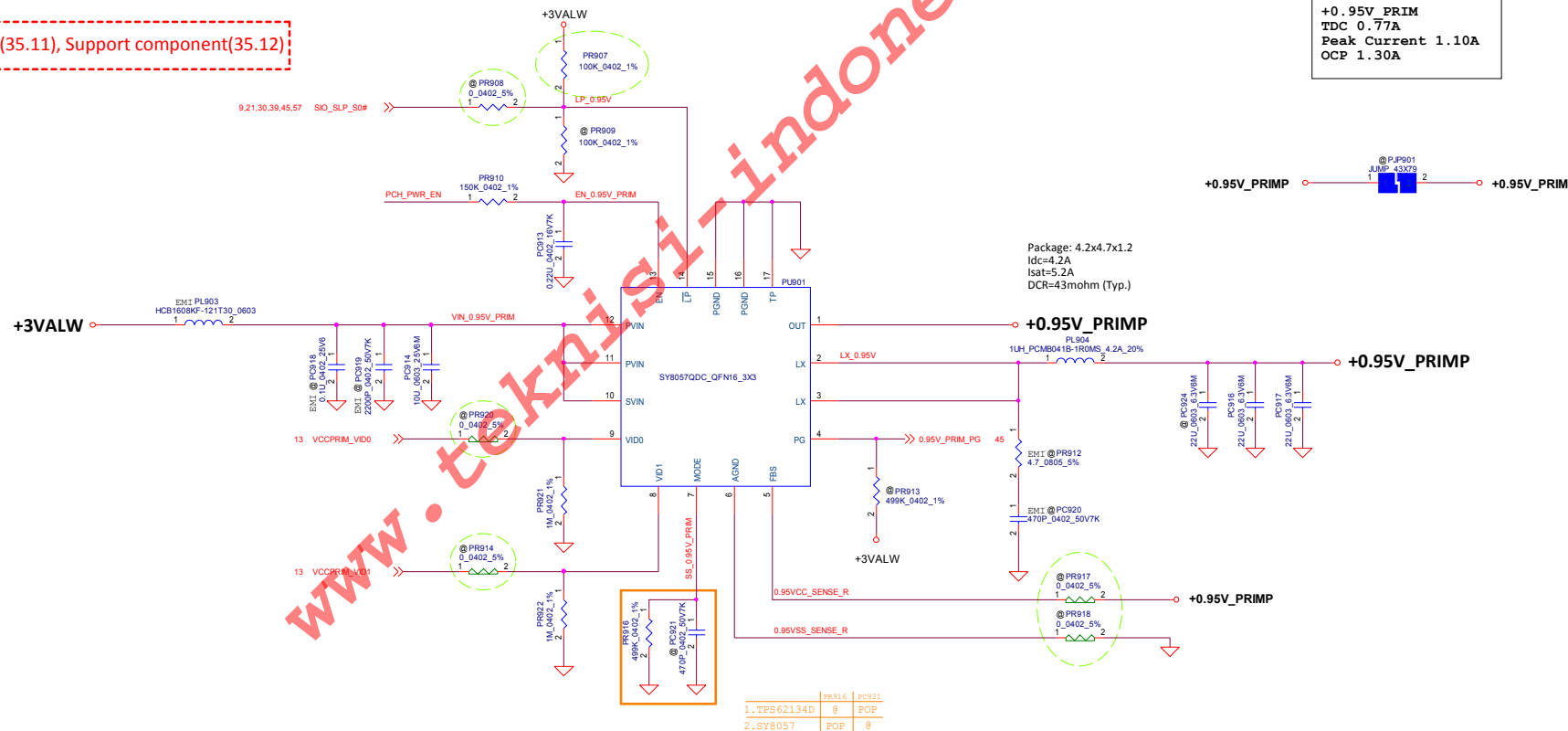


Security Classification	Compal Secret Data		Compal Electronics, Inc. P57-PWR +0.8VS VCCIO/4.10V PRIM	
Issued Date	2011/06/13	Deciphered Date	2012/06/13	Title Doc# Document Number Date# Date Friday, November 27, 2015
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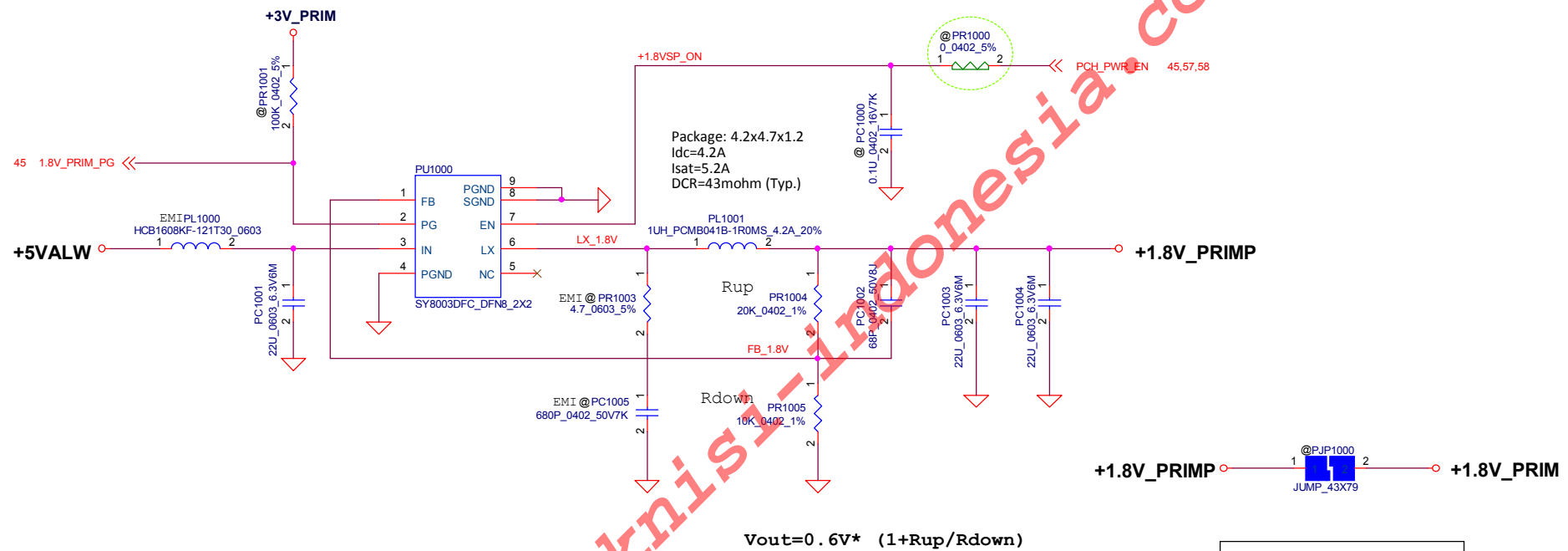
3V/5V controller(35.1), Support component(35.2)



+0.95V PRIM controller(35.11), Support component(35.12)



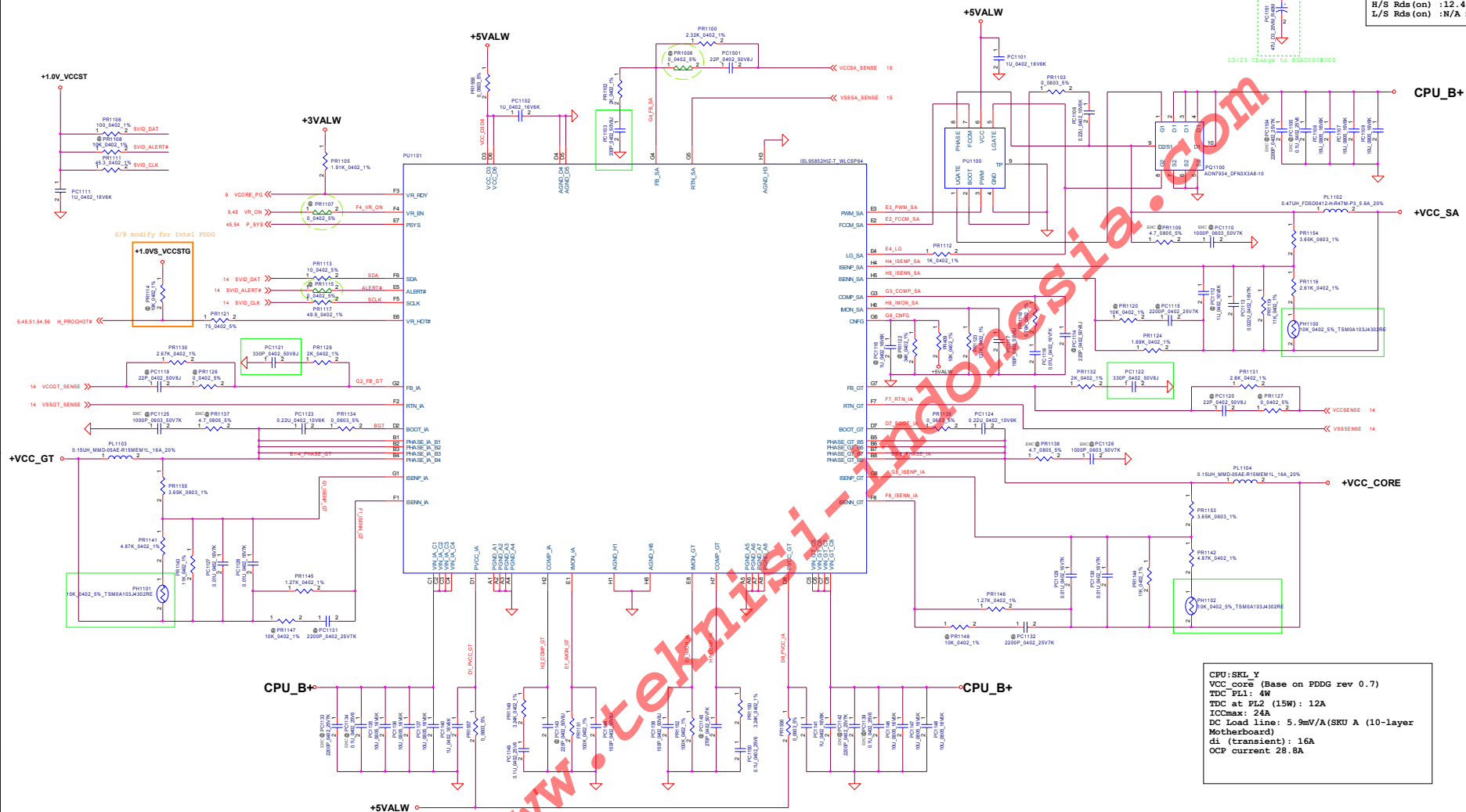
1.8V controller(35.15), Support component(35.16)



```
+1.8V PRIM
TDC 0.72A
Peak Current 1.04A
OCP 1.23A
```

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2011/06/13	Deciphered Date		2012/06/13	Title
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						Document Number
Date:				Friday, November 27, 2015	Sheet 59 of 66	

VCORE/GT/SA controller(36.1), Drivers(36.2), Support component(36.3)



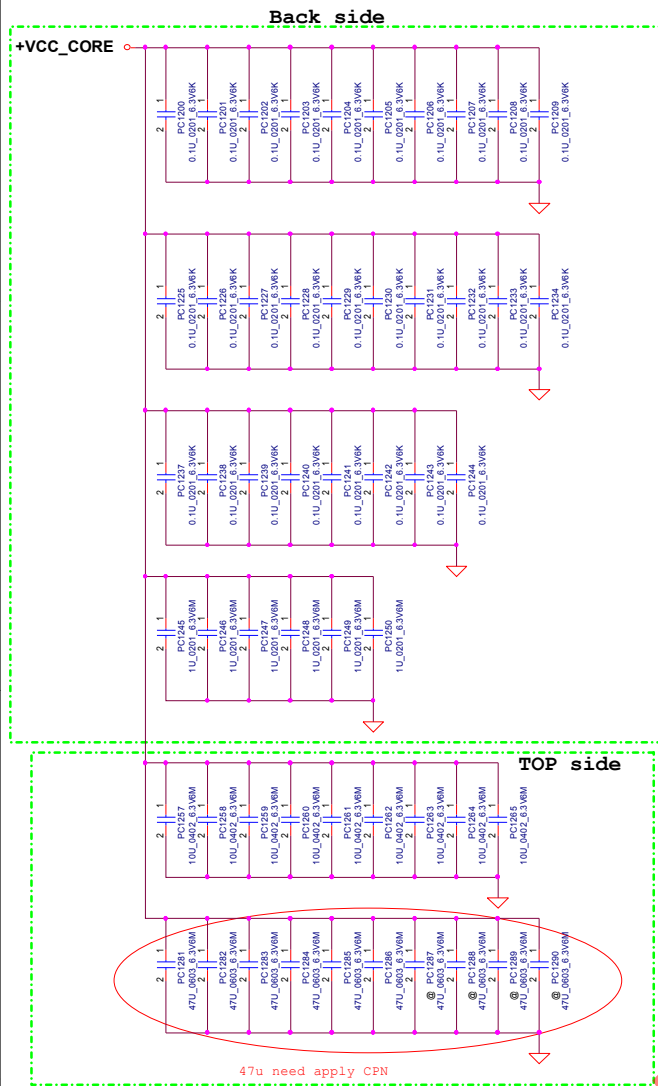
VCCGT:SKL_Y
VCC_GT (Base on PDDG rev 0.7)
TDC PL1: 4W
TDC at PL2: 11A
ICOMax: 24A
DC Load line: 5.7mV/A(SKU A (10-layer Motherboard))
di (transient): 20A
OCP current: 28.8A

VCCSA:SKL_Y
VCC_SA (Base on PDDG rev 0.7)
TDC PL1: 4W
TDC at PL2 (15W): 4A
ICOMax: 4A
DC Load line: 17.9mV/A(SKU A (10-layer Motherboard))
di (transient): 4A
OCP current: 6.97A

TYP MAX
H/S Rds(on) :12.4 mohm , 15.8 mohm
L/S Rds(on) :N/A mohm , 11.6 mohm

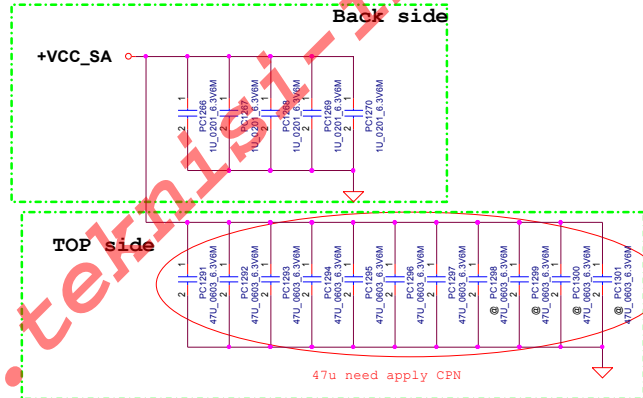
CPU:SKL_Y
VCC_core (Base on PDDG rev 0.7)
TDC PL1: 4W
TDC at PL2 (15W): 12A
ICOMax: 24A
DC Load line: 5.9mV/A(SKU A (10-layer Motherboard))
di (transient): 16A
OCP current: 28.8A

VCC CORE
0.1U_0201 * 28 pcs +1U_0201*6 pcs+10U_0402*9pcs+47U_0603*10pcs



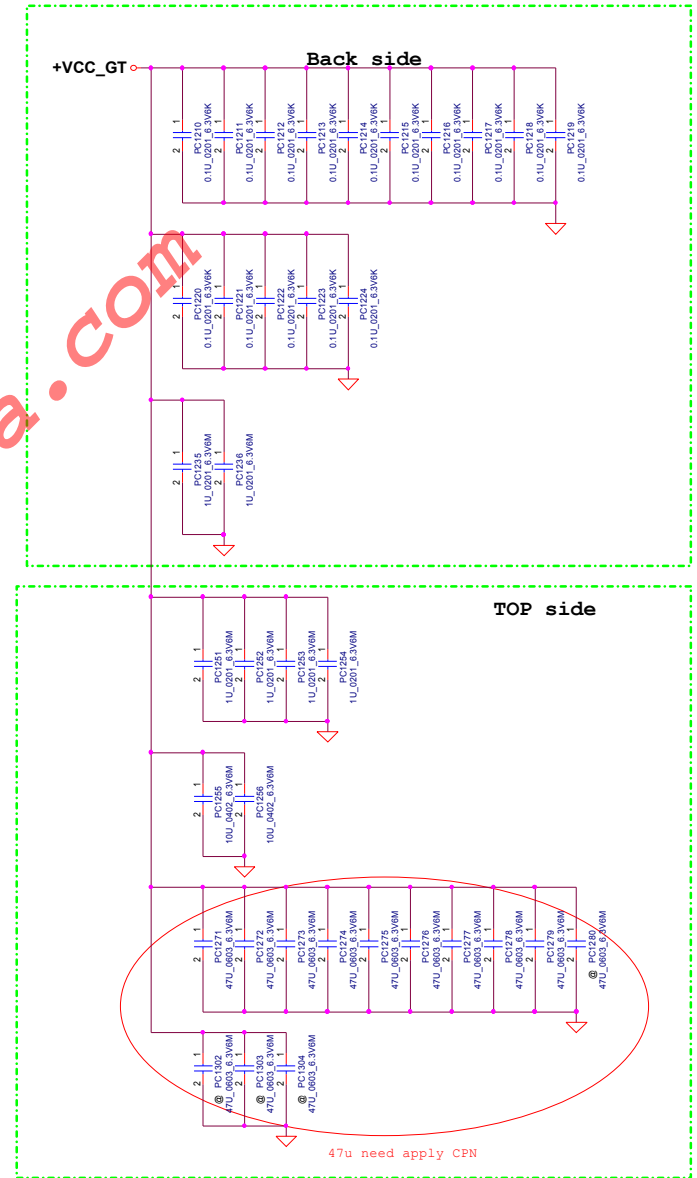
VCC_CORE output cap (36.4)

VCC SA
1U_0201 * 5 pcs +47U_0603*11 pcs

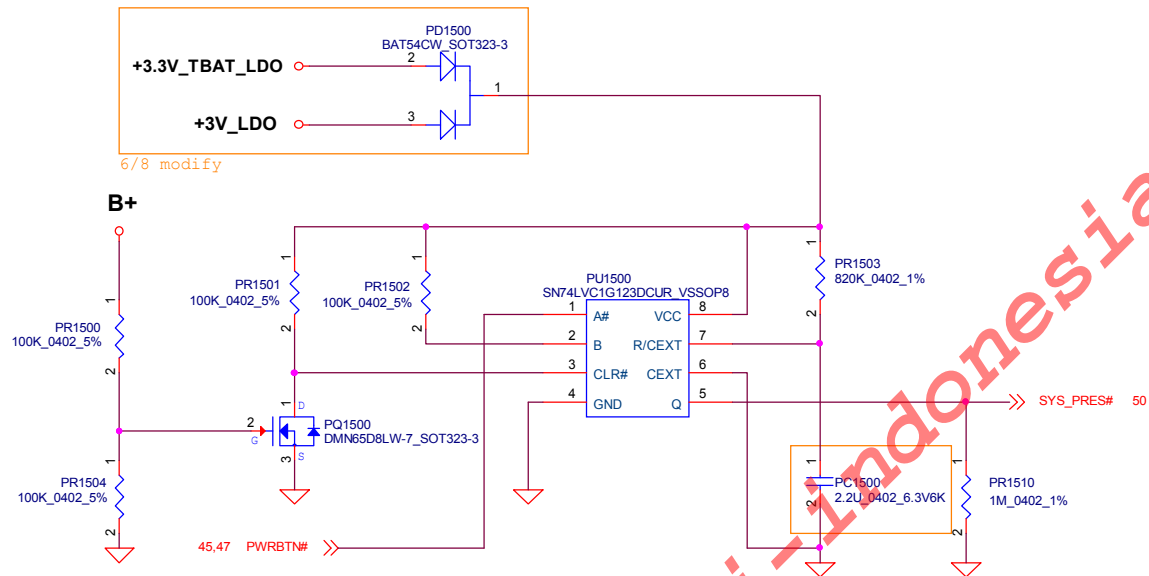


VCC_SA output cap (36.6)

VCC GT
0.1U_0201 * 15 pcs +1U_0201*6 pcs+1U_0402*4pcs+10U_0402*2pcs+47U_0603*13pcs



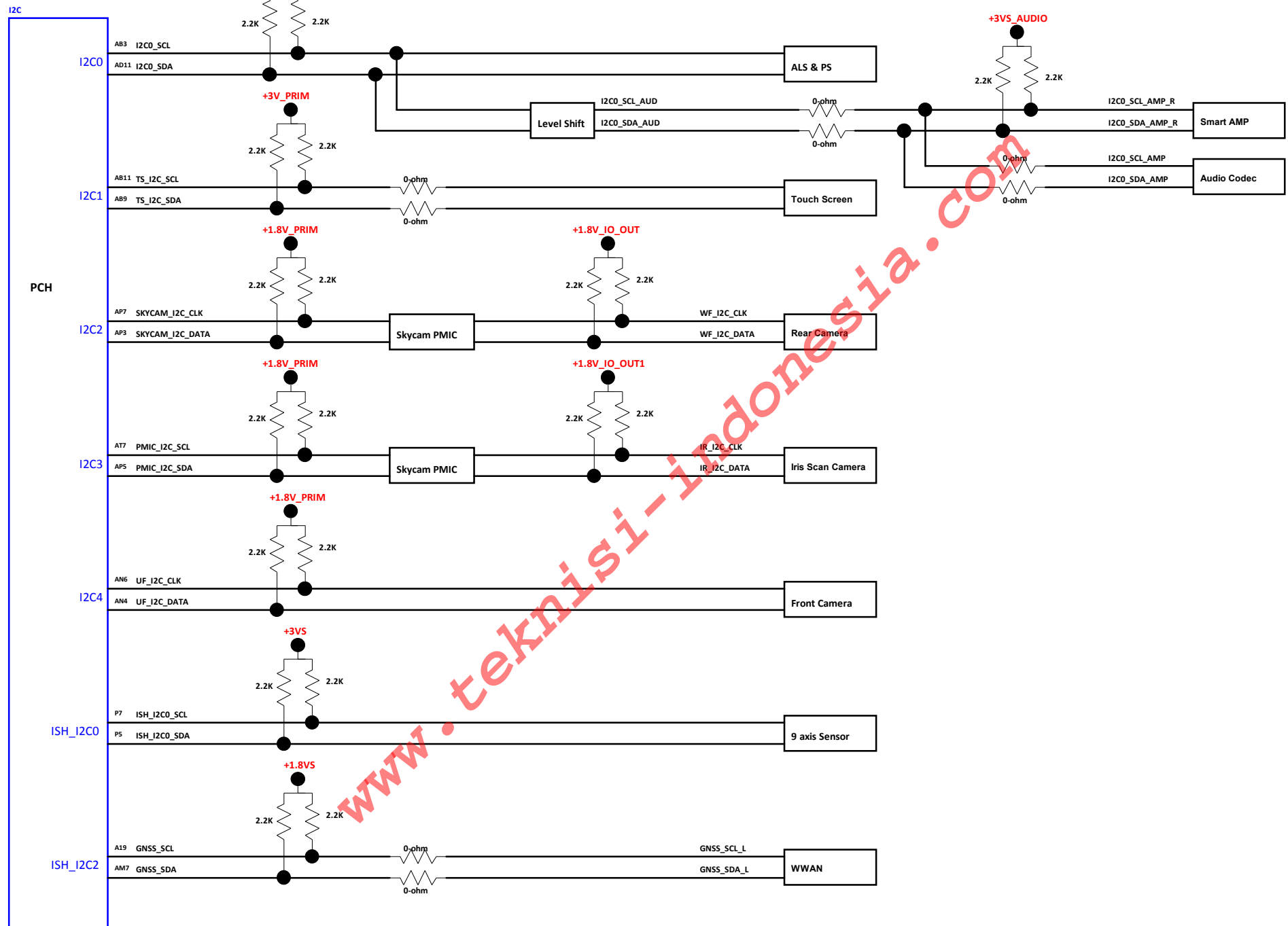
VCC_GT output cap (36.5)

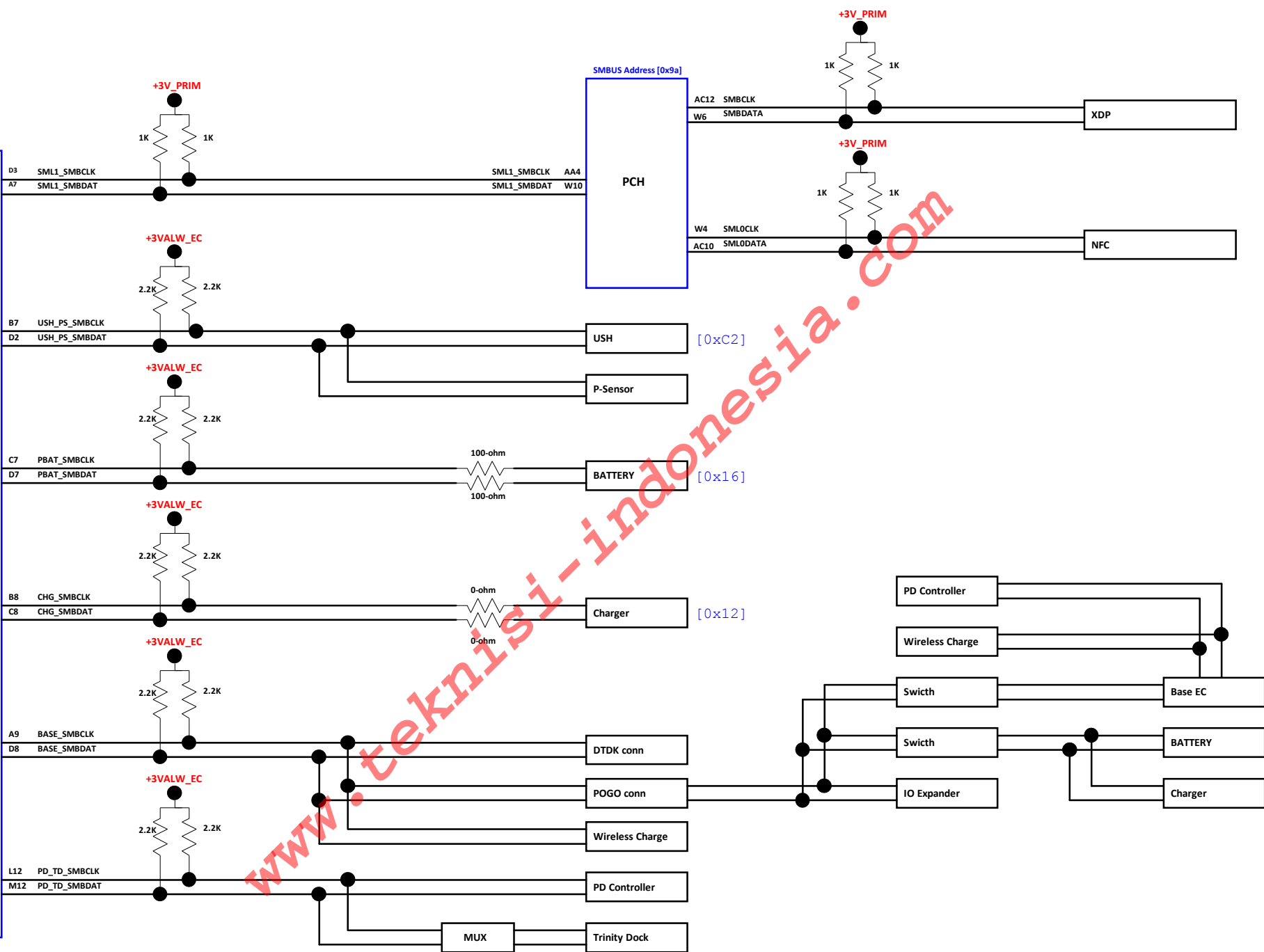
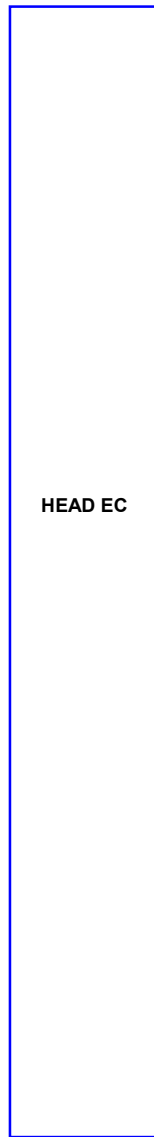


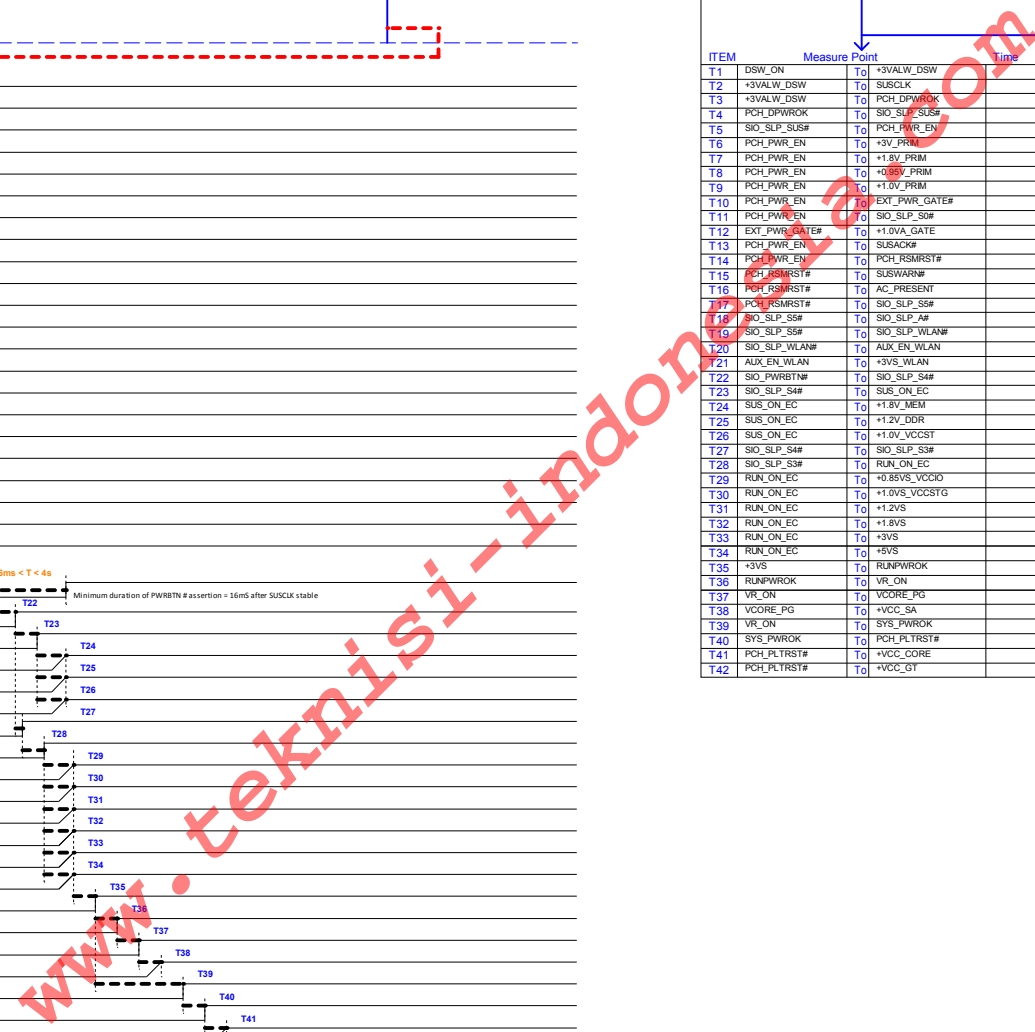
FUNCTION TABLE

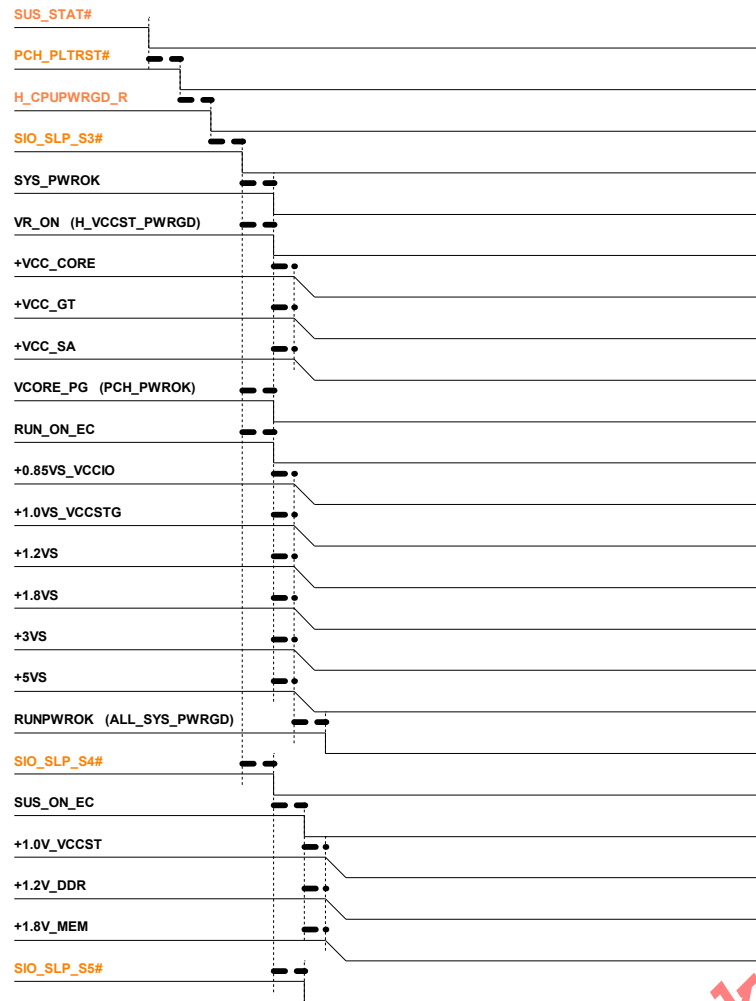
INPUTS			OUTPUTS
CLR	A	B	Q
L	X	X	L
X	H	X	L ⁽¹⁾
X	X	L	L ⁽¹⁾
H	L	↑	⌋
H	↓	H	⌋
↑	L	H	⌋

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Issued Date	2014/08/20	Deciphered Date	2015/08/20	Title	PWR POWER BLOCK DIAGRAM
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				Date: Friday, November 27, 2015	Sheet 62 of 66









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				Rev	1.0
				Date:	Friday, November 27, 2015
				Sheet	66 of 66